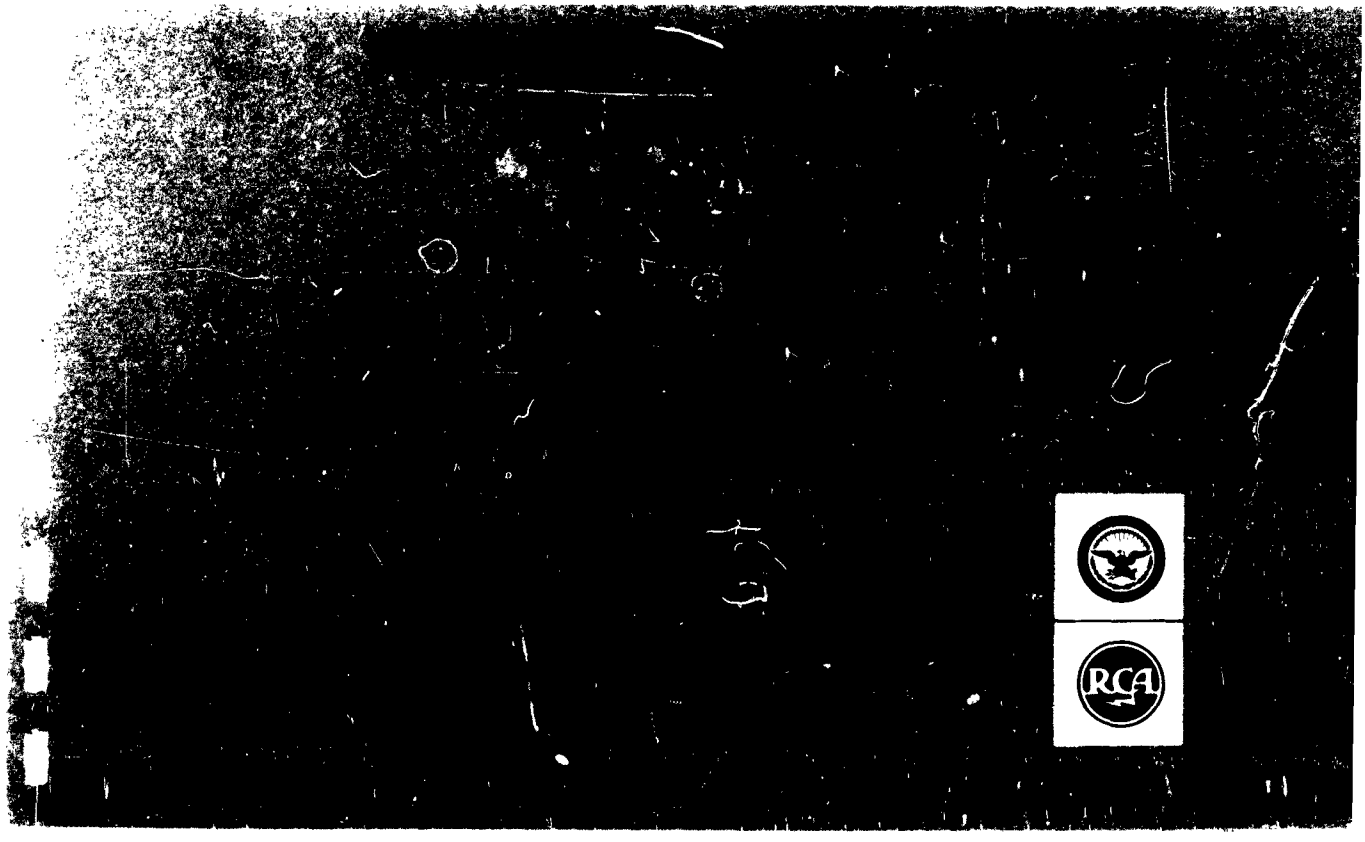
PROJECT

lightning



In accordance with RCA's letter of 27 May 1960 accepted by the Bureau of Ships in letter serial 687E-208 of 18 July 1960, and in letter serial 687E-294 dated 14 September 1960, the material contained in this report is not to be released for distribution by the Government prior to 31 March 1963.

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SUPPLEMENT TO

INTERIM RESEARCH REPORT NO. 15A

for

HIGH-SPEED DATA PROCESSOR SYSTEM RESEARCH

Project LIGHTNING

Prepared for
DEPARTMENT OF THE NAVY
Bureau of Ships, Electronics Division
Washington 25, D. C.
Contract Number - NObsr 77523, February 2, 1959
and Amendment Number 8 — June 27, 1960

Prepared by
Engineering Department
Electronic Data Processing
RADIO CORPORATION OF AMERICA
Camden, New Jersey

September 1, 1962

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Chapter 1. GENERAL

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1-1. INTRODUCTION

This supplemental report presents material not covered in the main cover of IRR-15A. The main topics are:

- Tunnel Device Research.
- The construction of the 40-gate subsystem.
- Task Supporting "Circuits and Fabrication Completions".

1-2. SUMMARY

A. TUNNELING DEVICES

The final work for Task IV of Phase III-B is reported herein. Several different methods of fabricating extremely small tunneling devices as individual elements were investigated. Samples were built.

B. LOGIC CIRCUIT DEVELOPMENT

All of the circuits to be incorporated into the 40-gate subsystem have been designed and tested in the laboratory. These circuits are essentially unchanged from that reported last period, with the exception that individual components have been design centered and the circuit simulation has been completed with worst-case times established on the RCA 301 Computer. Laboratory construction of prototype wafers embodying the three basic circuit types have shown the performance to agree with that predicted in the circuit simulation.

Very briefly, the worst-case individual delays are:

OR .6 nanosecond,

AND 1 nanosecond,

Bistable Set .65 nanosecond, and

Bistable Reset 1.1 nanoseconds.

It is interesting to note that the nominal times for these individual delays are in essential agreement with the original goals of LIGHTNING (.3 nanosecond logic level time). The worst-case repetition rates for these circuits are such as to allow 300-megacycle ring shift.

All components for the 40-gate subsystem have been ordered, and many were received. The most critical item of these is the tunnel resistor which is currently somewhat behind delivery schedule.

C. FABRICATION

The fabrication techniques for 40-gate subsystem construction are somewhat modified over those of the LIGHTNING Subsystem. This results in smaller overall physical size, higher packing density, and potentially cheaper cost. Samples have been received for the new I beams and the 12-pin wafer socket. A new coaxial signal connector has been designed in which the standing wave ratio is extremely small. All of the basic fabrication decisions have been made and specifications were frozen for construction of the 40-gate subsystem.

D. TASK IV - COMPLETIONS

Several circuit designs are underway as a portion of the circuit completions work. Design is nearing completion for the triggerable flip-flop, which has been tested. It is anticipated that the sum-of-products gate will operate with no increase in delay over that of the present AND gate. Pulse stretching circuits are also being designed.

In the area of fabrication, a three-dimensional frame stack is under study and some samples of frame-to-frame connectors have been built. The present 12-pin wafer socket appears adequate in the form supplied by the current vendors.

1-3. OBJECTIVES AND SCHEDULES

1. 40-Gate Subsystem

   (a) The wafers for this subsystem will be completed and tested.

   (b) These wafers will be assembled into the frame and the unit will be operated in its programmed mode.

2. The "Completions"

   (a) The design for the triggerable flip-flop will be completed and the circuit built.

   (b) A choice will be made as to the best approach for the pulse stretcher circuit and this design will be completed.

   (c) The sum-of-products gate will be designed and built.

   (d) A design for a three-dimensional frame stack will be completed.

   (e) The d-c distribution problem associated with three-dimensional stacks will be studied.

   (f) A choice will be made for the frame connector.

Chapter 2. 40-GATE SUBSYSTEM TECHNIQUES

SUMMARY

Three improved circuits have been designed for the 40-gate subsystem. Operation of these circuits will be demonstrated in a subsystem of approximately 40 wafers at the end of the next quarter. During this quarter, the design of the circuits were frozen, worst-case analyses were completed, and all components were specified as well as ordered for the subsystem. In addition, dynamic simulation of the circuits was continued using the RCA 301 Computer and worst-case delays determined from this simulation. To date, 6 subsystem wafers as well as 3 prototypes have been completed and tested. An additional 27 units are in the process of construction.

The performance of these individual circuits in the laboratory, in general, agrees with the simulated results.

A trimming test fixture has been designed and a procedure specified for trimming each type of gate.

Work has started on triggerable flip-flop circuits and pulse stretching circuits to complement the 40-gate subsystem circuits.

Chapter 2. 40-GATE SUBSYSTEM TECHNIQUES

I. PERSONNEL

The following personnel contributed to this phase of the project during the fifteenth quarter.

I. Abeyta
R. H. Bergman
M. Cooperman
E. C. Cornish
D. R. Crosby
M. E. Ecker
H. R. Kaupp
W. J. Lipinski
C. Pendred
H. Ur
R. D. Yates

II. DISCUSSION

A. LOGIC CIRCUITS

The final design and theoretical evaluation of the 40-gate subsystem logic circuits has been completed. Following is a description of their operating mode, design and performance.

1. Circuit Operation

a. Basic Monostable Stage

The basic monostable stage, which consists of a tunnel diode in series with an inductance and a tunnel resistor, is shown in Figure 2-1. The tunnel resistor is a new device formed by plating a resistive path across a tunnel diode junction. The two are then mounted in one glass package to form one device. (The process of plating and mounting in one package is used in order to keep the stray inductance between the two elements to a minimum. Otherwise the tunnel diode may oscillate, thus preventing the two elements from acting as one device). The characteristic of a tunnel resistor and the elements from which it is formed are shown graphically in Figure 2-2. The characteristic of a tunnel rectifier is shown in Figure 2-3.

To facilitate describing the operation of this circuit, the tunnel resistor biasing characteristic superimposed on the characteristic of the tunnel diode was plotted in Figure 2-4. (The more popular term for "biasing characteristic" is "load line". However, since this circuit will have other loads, the term "biasing characteristic" is preferred.) When an input is applied to the stage of Figure 2-1, the biasing characteristic shifts to a position indicated by curve b in Figure 2-4. This causes switching along the trajectory indicated by the dotted lines. The switching

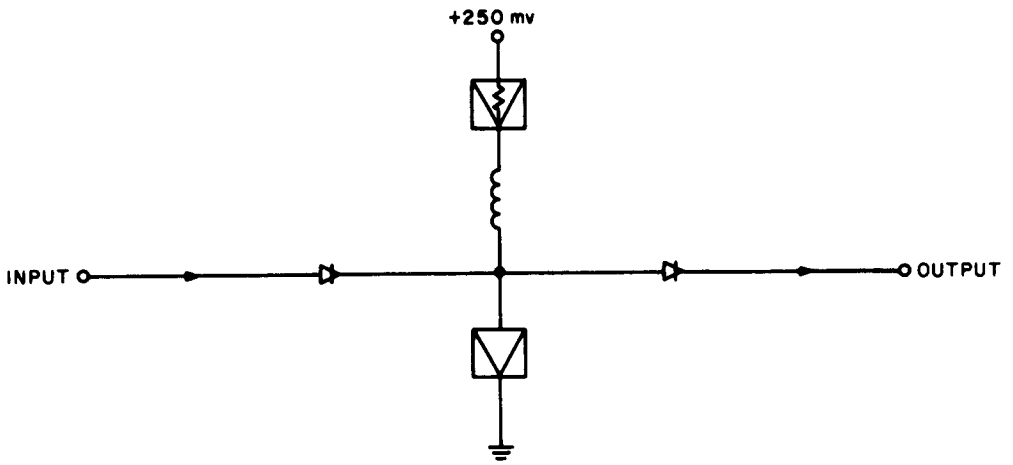


Figure 2-1. Basic Monostable Stage [5]

cycle is divided into a number of regions as indicated in Figure 2-4. The tunnel resistor provides a desirable biasing characteristic as it is relatively flat when the tunnel diode switches over the peak; it then drops sharply to permit monostable operation. Since the voltage required to obtain this biasing characteristic is only 250 mv, the power dissipation of the stage is relatively low. (See Table 2-1).

b. Tunnel Diode OR Gate

To perform a logical OR function, a circuit must produce an output when any one of its inputs is activated. This is easily accomplished by providing more than one input to the basic monostable stage of Figure 2-1. A current into any one of the inputs causes the tunnel diode to fire and thus accomplishing an OR operation.

A complete circuit diagram of a tunnel diode OR gate is shown in Figure 2-5. It consists of two monostable stages cascaded to provide the required current amplification. (TD_1, TDR_1, R_1 and L_1 are elements of the first stage, while TD_2, TDR_2, R_2 and L_2 are elements of the second stage.) Due to the requirements of increased fan-in, fan-out and speed, new techniques had to be employed in this circuit. Two of the most important circuit techniques now utilized in the OR gate and the other gates are "Trimming" and "Transmission line terminating".

Trimming is accomplished with R_1 and R_2; transmission line termination is accomplished by a network consisting of TR_1 and TR_2. Both of these techniques are described below.

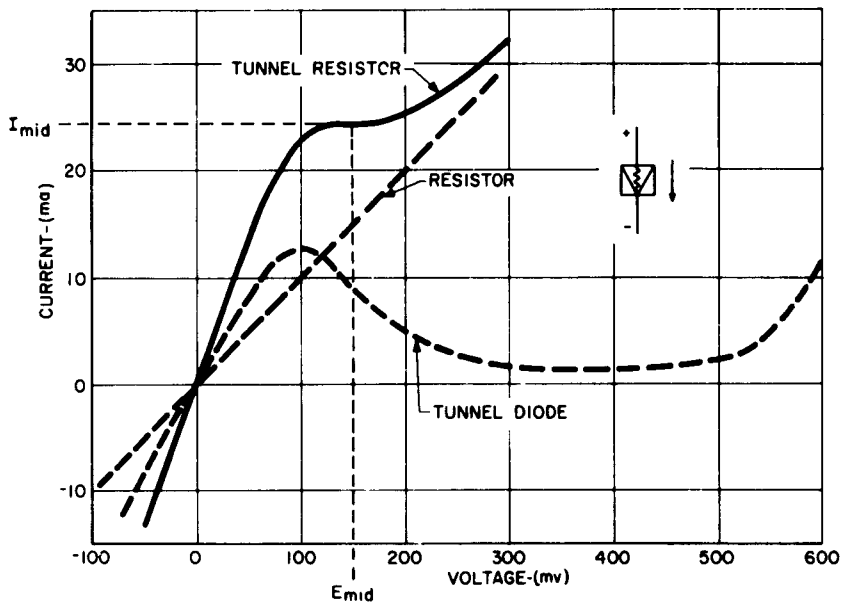


Figure 2-2. Graphical Construction of Tunnel Resistor Characteristic [a]

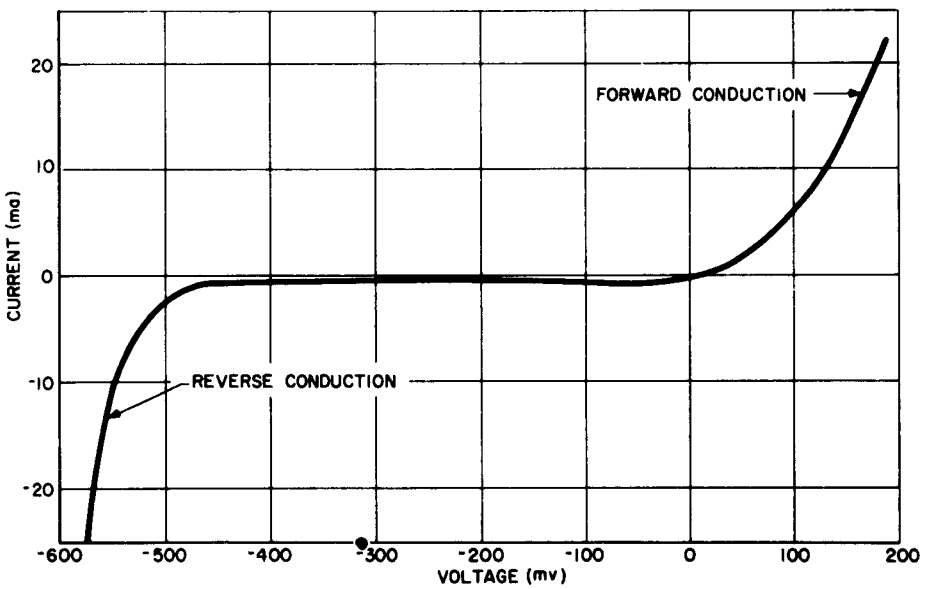


Figure 2-3. Tunnel Rectifier Characteristic [a]

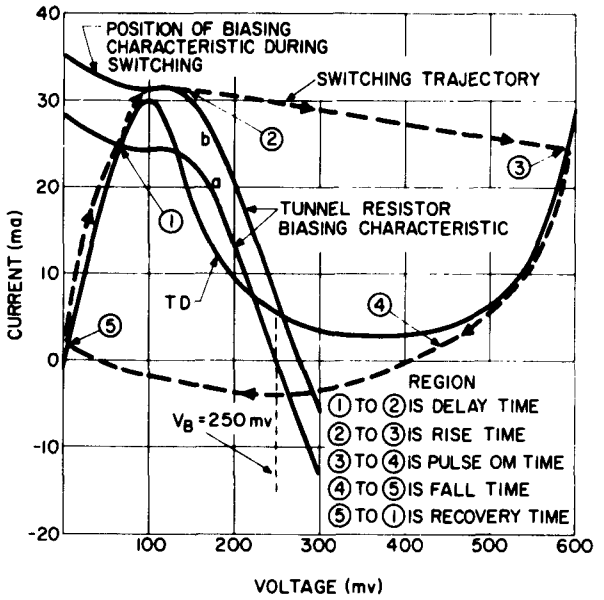


Figure 2-4. Graphical Representation of Monostable Stage With Tunnel Resistor Biasing [5]

(1) Trimming

In order to increase both fan-out and operation speed, TD_1 and TD_2 (Figure 2-5) required being biased closer to their peaks. However, worst-case tolerance conditions do not permit this. In order to cancel some of these tolerance variations, a current source of several milliamperes is added to each stage. In Figure 2-5, the current sources for the first and second stages are provided by R_1 and R_2 connected to +3 volts. The resistance of R_1 and R_2 is increased by trimming (mechanically removing some of the conductive material). After the gate is assembled, R_1 and R_2 are adjusted in accordance with a specified procedure to bias each stage to the desired amount below its tunnel diode peak. R_1 and R_2 are called trimming resistors. In addition to its essential functions, trimming also provides the desirable characteristic of making the electrical performance more uniform. This results in an additional increase of speed in the entire system.

(2) Terminating Network

The purpose of the terminating network is to eliminate reflections between gates. The operation of this network may be understood by referring to Figure 2-6 which shows an output stage of an OR gate driving the input stage of an OR gate via a transmission line. When TD_2 fires it supplies a current to TD_1 via TR_0, TR_i and TR_2. TR_1 is biased so that during this time it absorbs no current. When TD_1

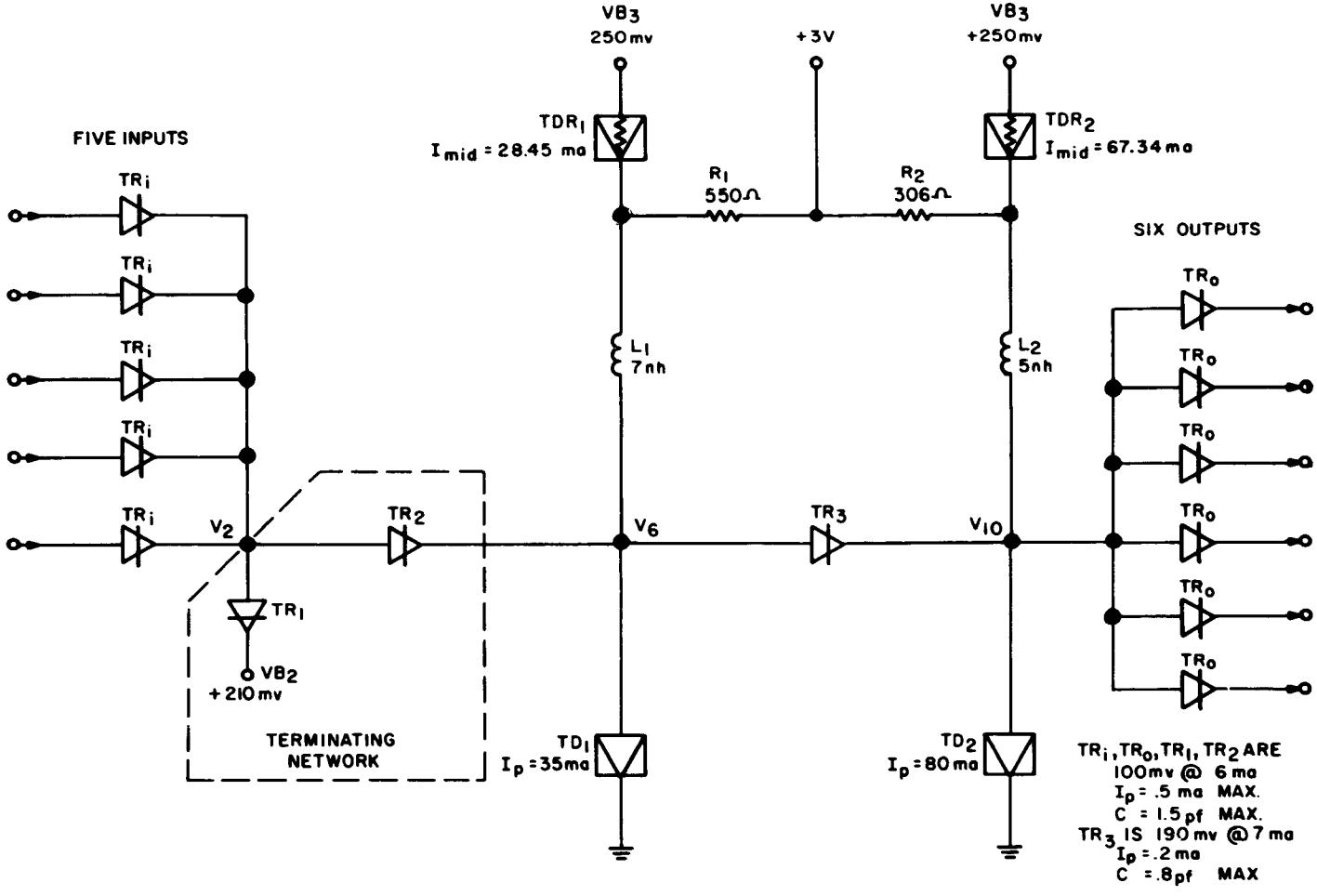


Figure 2-5. Tunnel Diode OR Gate (s)

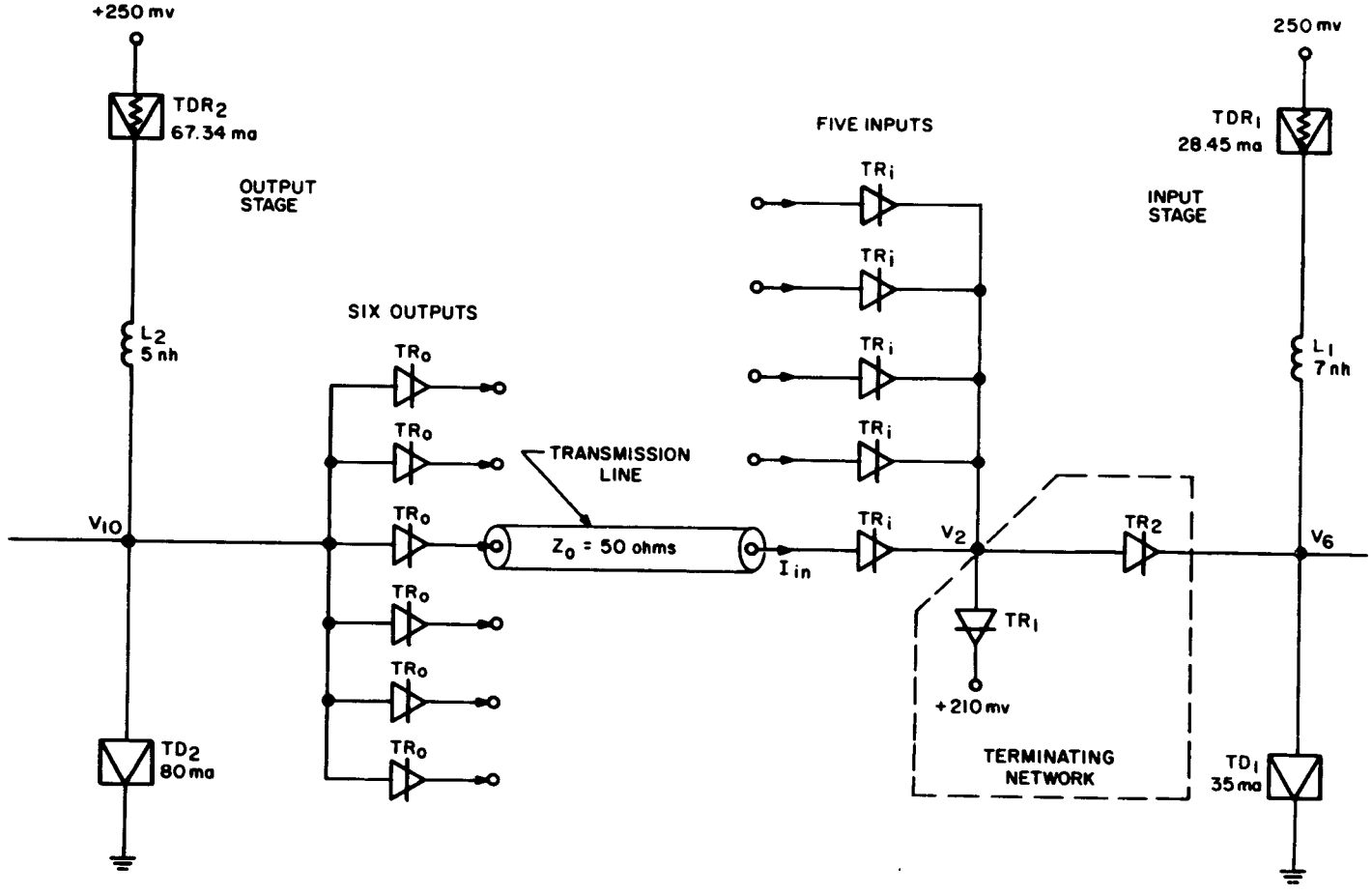


Figure 2-6. Interconnection of Gates (s)

fires, V_6 increases to about 500 mv. This rise in voltage prevents input current I_{in} from flowing and would, if TR_1 were not in the circuit, be reflected to its source. Depending on the length of the transmission line and the pulse width produced by TD_2, this current may once again be reflected. By this time the current pulse is traveling towards the input stage and if that stage had recovered from its firing cycle, this reflection could cause undesired firing of TD_1. With TR_1 in the circuit, current I_{in} is absorbed by TR_1 when TD_1 fires the first time. Thus the flow of I_{in} is practically not interrupted, and consequently no reflection is generated. The characteristics of TR_i, TR_1 and TR_2 are chosen such that the transmission line will be approximately terminated at all times.

In the preceding description the arrival of one input only has been considered. However, the gate has a fan-in of five and if all five inputs arrive at the same time the input current becomes five times as large (30 ma). If the resistance of TR_1 in the conductive region was low enough all five inputs could be terminated at all times. However, for presently available tunnel rectifiers, the resistance is too high. Under these conditions only 60% of the total current of the five inputs can be terminated. In order to be able to tolerate the remaining reflection, the maximum length of transmission line connections between monostable gates is restricted to the previously specified 6 inches. This guarantees that no reflection will arrive at TD_1 after it has recovered and is ready to be fired again. The terminating network is essential, even though it only terminates partially. If no terminations were present, the maximum transmission line restriction would have to be reduced to an impractically short length due to the high fan-in and fast recovery of the gates.

Other advantages obtained from the terminating network are:

(a) Since the terminating network absorbs the input current when it cannot flow into TD_1, the input of the gate becomes effectively a constant load for the output of the driving gate. This feature is utilized in designing the output stage to operate at the required repetition rate.

(b) Any leakage current due to the inputs must go through TR_2 when going into or out of TD_1. Since the d-c impedance of TR_2 is about six times that of TD_1, these leakages are considerably lower than if the inputs were connected directly to TD_1.

c. Tunnel Diode AND Gate

A schematic diagram of the AND gate is shown in Figure 2-7. In order to understand the operation of this gate, it is divided into three stages: pulse buffer stage, AND stage and output stage. All of these stages operate in a monostable mode and are biased with tunnel resistors as in the OR gate.

The AND gate is designed to operate as follows:

A pulse input, after being reshaped by the pulse buffer stage, is applied to TD_2 of the AND stage.

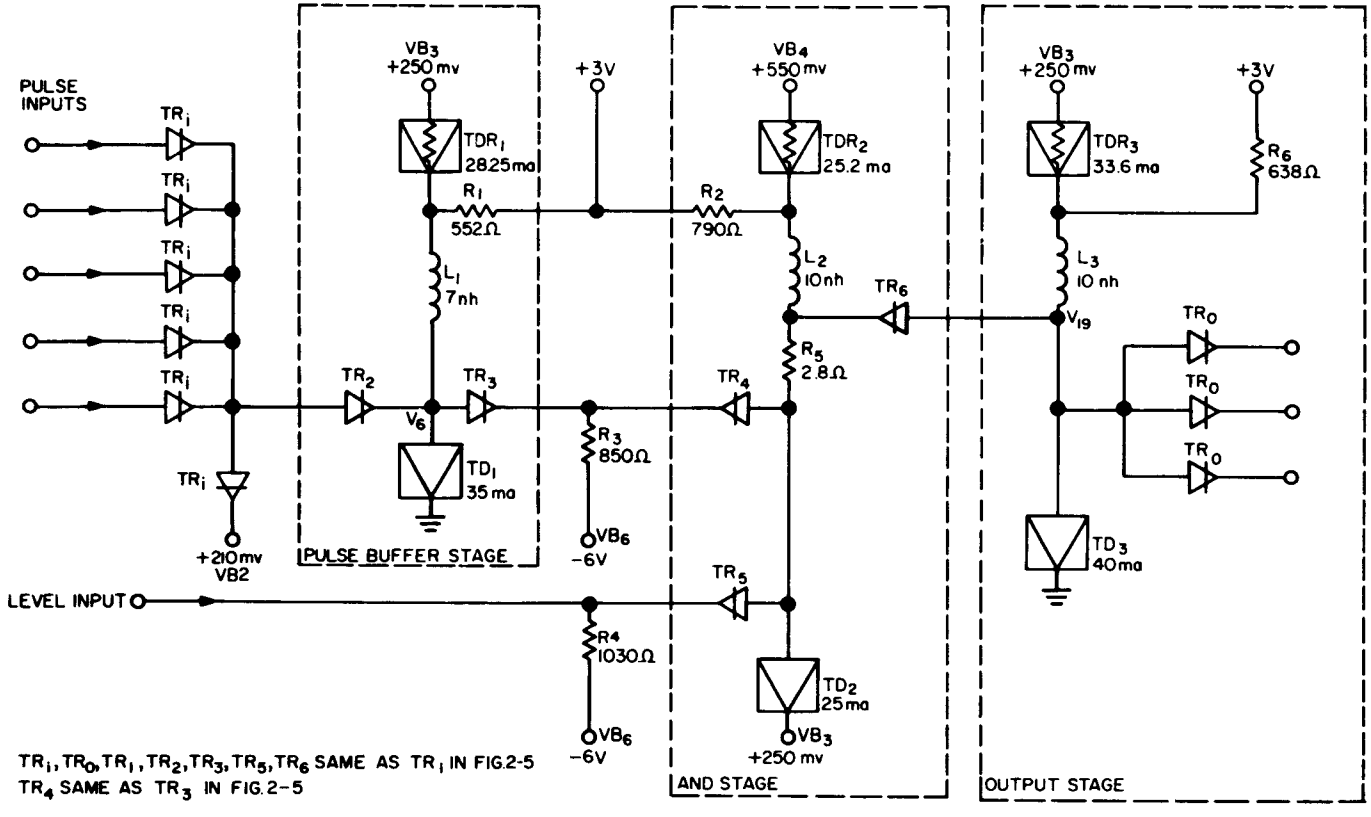


Figure 2-7. Tunnel Diode AND Gate [s]

TD_2 is returned to a positive potential so that under quiescent conditions TR_4 and TR_5 are conducting currents the amplitudes of which are determined by the magnitudes of R_3 and R_4, respectively. If either the pulse or the level is low, the AND stage is inhibited from firing due to the conduction of either TR_4 or TR_5. The presence of a level cuts off TR_5 while an output from the pulse buffer stage cuts off TR_4. This causes the entire current from TDR_2 to flow into and fire TD_2.

This type of AND gate has the advantage of not requiring tight control between the amplitude of its pulse and level inputs. The only requirement is that the inputs (V_6 and V_L) be less than 100 mv when they are low and greater than 470 mv when they are high.

(1) Output Stage

The output stage is coupled to the AND stage via the reverse direction of TR_6, the characteristic of which is shown in Figure 2-3. Coupling in this manner is necessary in order that the quiescent voltage difference (approximately 250 mv) between the AND stage and output stage be absorbed with negligible d-c leakage current between the two stages.

The purpose of R_5 is to provide the proper biasing characteristic for the AND stage and efficient coupling between the AND and output stages.

(2) Pulse Buffer Stage

This stage serves several important functions:

(a) It converts the pulse input impedance of the AND gate to that of the other gates. This prevents the AND gate from imposing severe requirements upon the preceding gate, alleviating a reduction in fan-out of all gates.

(b) It makes the pulse input impedance of the AND gate compatible with the termination network used in the OR gate.

(c) The output of the buffer stage is relatively insensitive to input pulse width variations. Thus under all conditions of input, the buffer stage generates a narrow pulse of constant width. This reduces the waiting period for applying a level after the application of a pulse.

In this gate, trimming is employed whenever possible. R_1, R_2 and R_6 are the trimming resistors for the buffer, AND and output stages, respectively.

d. Tunnel Diode Bistable Circuit

The bistable circuit consists of a set amplifier, inverter driver, inverter and bistable unit as shown in the block diagram of Figure 2-8.

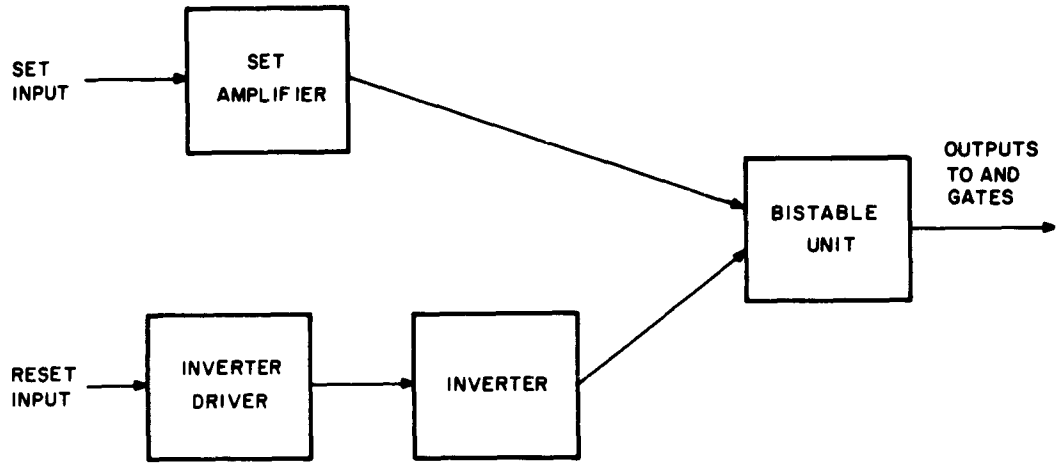


Figure 2-8. Bistable Circuit Block Diagram (5)

The bistable unit stores a "0" when it is in the low state and a "1" when it is in the high state. The other units are monostable and when activated their function is to set or reset the bistable unit.

A schematic of the bistable circuit is shown in Figure 2-9. The bistable unit consists of TD_4, V_{B4}, V_{B6} and R_4. Bistable action is obtained in conjunction with the AND gate loading as is illustrated in Figure 2-10. After the curve of TD_4 is inverted and returned to 550 mv, its characteristic shifts from the first into the fourth quadrant. The current biasing characteristic of R_4, in conjunction with that of the AND gate input characteristic, results in a bistable load line as indicated.

(1) Setting

The set amplifier is a monostable stage identical to the first stage of an OR gate. When activated by a set pulse, the set amplifier supplies an amplified current pulse to the bistable unit which is switched to the high state along the indicated trajectory of Figure 2-10.

(2) Resetting

The inverter driver which consists of TD_2 and TDR_2 operates like a monostable stage whereas the inverter, consisting of TD_3 and TDR_3, is an inverted monostable stage.

When a reset input is applied, TD_2 switches to the high state. This causes the current (I_2) in TD_2 and TDR_2 to decrease. A decrease in I_2 acts as a negative current input into TD_3, triggering the inverter to produce a negative pulse.

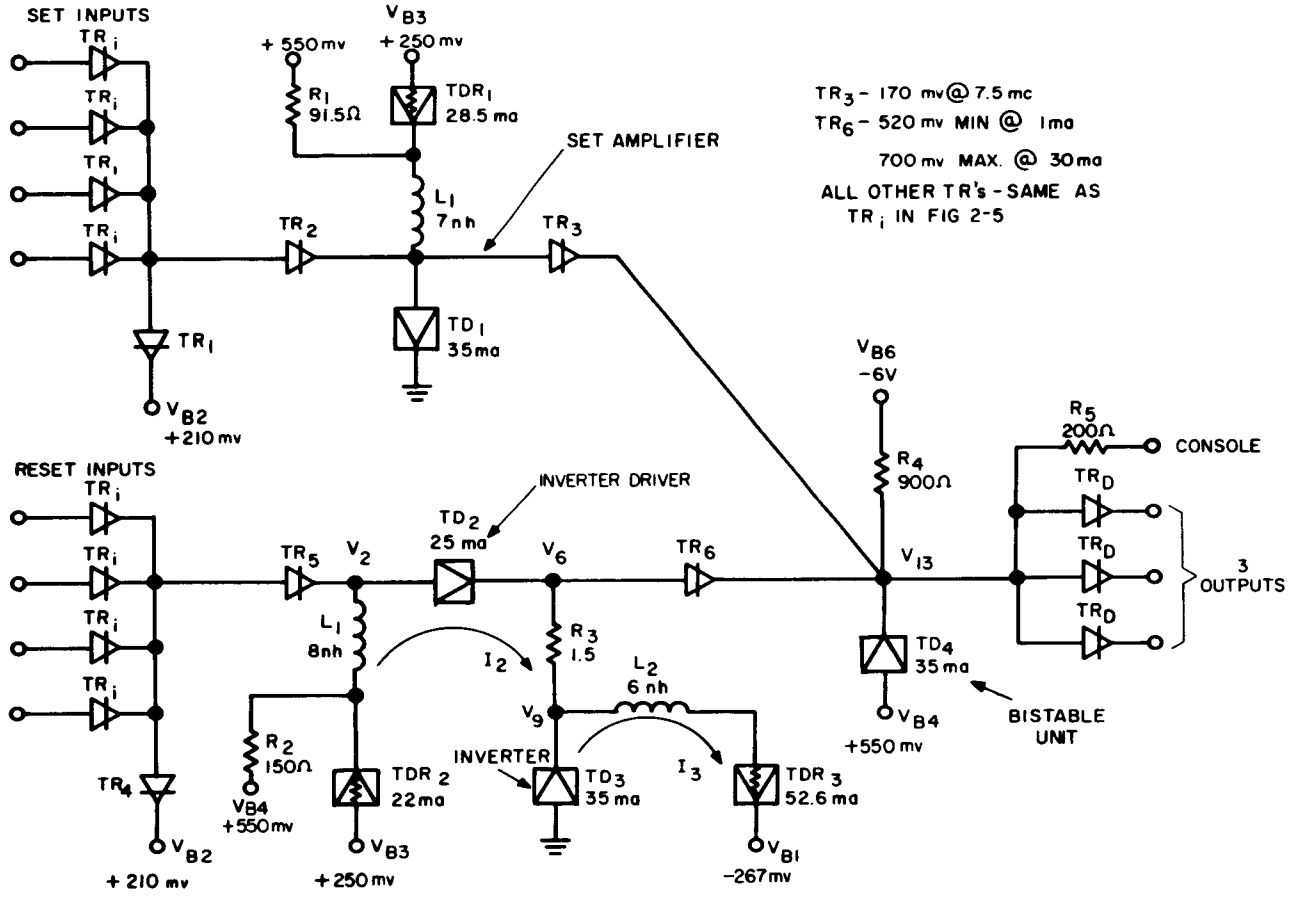


Figure 2-9. Tunnel Diode Bistable Circuit [s]

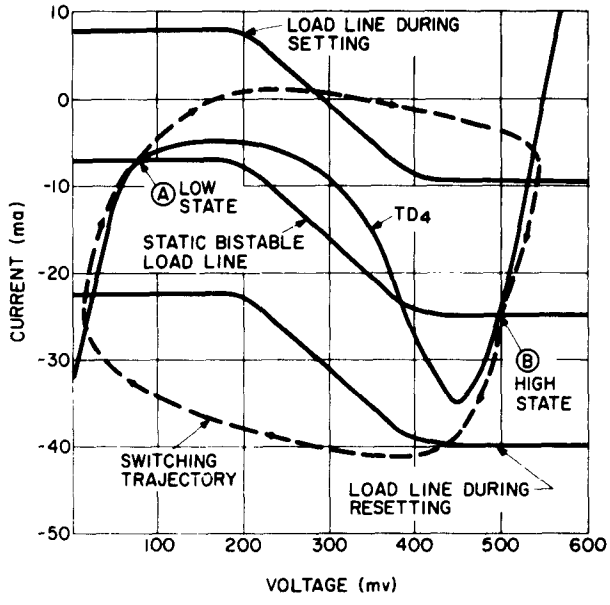


Figure 2-10. Graphical Representation of Bistable Switching [5]

The negative pulse causes reverse conduction in TR_6 which diverts some of the current from TD_4. (An approximate characteristic for TR_6 is shown in Figure 2-3). A current flowing out of TD_4 causes the load line of Figure 2-10 to move down such that the intersection at point B dissappears. This causes the bistable unit to switch to the low state along the indicated trajectory.

This circuit configuration, where the bistable diode is inverted and returned to a voltage source, has several advantages over the previously used bistable circuit.

Here, since resetting is accomplished from the peak which is considerably narrower than the valley, the reset requirements are reduced. Thus no inductance is required in the bistable load line, permitting a faster level current change and higher repetition rate.

Setting the circuit is somewhat more difficult since switching is done from the valley. This disadvantage is partly offset by the fact that this circuit can operate quiescently closer to the valley. Also more setting current can be made available without sacrificing operating speed.

In this bistable circuit, resistors R_1 and R_2 are used to trim the set amplifier and inverter driver, respectively. The purpose of R_3 is to boost voltages V_2 and V_6 to a value required for proper operation.

2. Circuit Performance

Table 2-1 summarizes the circuit properties and performance. Following is a definition of the terms used in the table:

Delay — This is the total delay of the gate from input to output. It is measured at the 300 mv points.

Repetition Rate — Maximum repetition rate at which clock pulse may be applied.

T_1 Waiting time between the application of a pulse and application of a level to an AND gate when switching is desired.

T_2 Waiting time between application of a pulse and application of a level to an AND gate when switching is not desired.

T_3 Waiting time between the application of a pulse and the removal of a level from an AND gate when switching is desired.

T_4 Waiting time between the application of a pulse and the removal of a level from an AND gate when switching is not desired.

Set-Reset — Waiting time between the application of a set pulse and the application of a reset pulse to a bistable gate.

Reset-Set Wait — Waiting time between the application of a reset pulse and the application of a set pulse to a bistable gate.

TABLE 2-1
GATE PROPERTIES AND PERFORMANCE

OR	Fan-in	5
	Fan-out	6
	Delay	.27 ns min - .6 ns max
	Repetition rate	300 mc
	D-C Power Dissipation	57 milliwatts

TABLE 2-1 (Cont.)
GATE PROPERTIES AND PERFORMANCE

AND	Fan-in	6 (5 pulse and 1 level*)
	Fan-out	3
	Delay	.65 ns min - 1.00 ns max
	Repetition rate	300 mc
	$T_1 \leq$	.13 ns
	$T_2 \geq$	1.00 ns
	$T_3 \geq$	.62 ns
	$T_4 \leq$	.13 ns
	D-C Power Dissipation	137 milliwatts
BISTABLE	Fan-in set	4
	Fan-in reset	4
	Fan-out	3 + Console
	Set Delay	.13 ns min - .65 ns max
	Reset Delay	.23 ns min - 1.1 ns max
	Set-Reset Wait $\geq$	1.6 ns
	Reset-Set Wait $\geq$	2.0 ns
	Repetition Rate	150 mc
	D-C Power Dissipation	74 milliwatts

* performs an AND operation between the level and any one or more of the five pulse inputs

3. Design Considerations

The three circuits were designed to operate under worst-case conditions of component and power supply variations. Table 2-2 lists the tolerance variations in components and power supplies. Additional information on components and their tolerances are provided in Figures 2-5, 2-7 and 2-9.

The choice of circuit parameters was based on d-c worst-case analysis and dynamic simulation on the RCA 301 Computer.

TABLE 2-2
COMPONENT AND POWER SUPPLY TOLERANCES

Parameter		Symbol	Tolerance Variation (Initial + Aging)
Tunnel Diode Peak Current		I_P	±2%
Tunnel Diode Peak Voltage		E_P	±5%
Tunnel Diode Valley Voltage		E_V	390 mv min
Tunnel Diode Voltage @ $I = I_P$		E_f	±5%
Tunnel Resistor Current in Flat Region		I_{mid}	±2.5%
Resistors		R	±2%
Inverter Bias	(-267 mv)	V_{B1}	±10 mv
Termination Network Bias	(+210 mv)	V_{B2}	±10 mv
Tunnel Resistor Bias	(+250 mv)	V_{B3}	±10 mv
Bistable Bias	(+550 mv)	V_{B4}	±10 mv
Trimming Voltage	(+3,000 mv)	V_{B5}	±2%
AND Gate Current Source Supply	(-6,000 mv)	V_{B6}	±2%

a. OR Gate

In the design of the OR gate, a fan-in of 5 and a fan-out of 6 was required. This gate was designed in accordance with following equations:

$$I_B \text{ max} \leq I_P \text{ min} - I_s - I_{Lin} \quad (1)$$

$$i_{in} \text{ min} \geq I_P \text{ max} - I_B \text{ min} + I_o + I_{Lout} \quad (2)$$

where:

I_B is the nominal bias current

I_{Lin} is the total leakage current into the diode when switching is not desired.

I_{Lout} is the total leakage current out of the diode when switching is desired.

I_o is the minimum overdrive current when switching is desired.

I_P is nominal peak current of the tunnel diode

I_s is the safety current when switching is not desired

i_{in} is the input current.

Some of the significant calculated values for the first and second stages of the OR gate are given in Table 2-3 below:

TABLE 2-3
CALCULATED CURRENTS FOR OR GATE

Parameter Symbol	First Stage	Second Stage
I_P	35 ma	80 ma
$I_{BP\ max}$	3.75 ma	8.5 ma
$I_{BP\ min} = I_s$	1.5 ma	3.0 ma*
I_{Lin}	.3 ma	.78 ma
I_{Lout}	0 ma	.18 ma
I_o	1.7 ma	4.0 ma
i_{in}	5.45 ma	12.36 ma

* The safety factor for the second stage of the OR gate is large enough to tolerate the capacitive feed through of three of its outputs.

IBP is the bias below the peak of the tunnel diode with leakage currents included. Some of the significant voltage variations with no inputs or outputs connected are:

V_6 = 64 mv to 79 mv

V_{10} = 65 mv to 81 mv

The current available from the output stage under worst-case condition was calculated from dynamic operation with the 301 Computer. In order to obtain a minimum current of 36 ma (to supply six outputs of 6 ma each), a tunnel diode having an I_P = 80 ma had to be used. The high ratio of I_P to output current is due to the high stray inductance (1 nh) of the tunnel diode. A circuit model used to study the dynamic behavior of the OR gate driving six other gates is shown in Figure 2-11. The initial conditions in this model were chosen to produce maximum delay and worst-case operating conditions. TR_1 represents the series combination of the input TR to this gate and the output TR of the preceding gate. Resistors R_1 and R_2 are used to simplify programming of the circuit. Their value is chosen sufficiently high so as not to effect the results. Some of the most significant voltage and current waveforms of this circuit are shown in Figures 2-12 and 2-13. The operation of the termination network can be seen by observing the voltages at V_2 and V_3.

b. AND Gate (Figure 2-14)

The AND gate was designed to have a fan-out of five pulses into the buffer stage, which is the same as the first stage of the OR gate. The buffer stage supplies a pulse to the AND stage which is then gated against the level. The AND stage was designed in accordance with the following equations:

$$I_{L1} + I_{B\,max} - i_{L\,min} \leq I_{P\,min} - I_{SP} \quad (3)$$

$$I_{L2} + I_{B\,max} - i_{P\,min} \leq I_{P\,min} - I_{SL} \quad (4)$$

$$I_{B\,min} - I_{Lout} \geq I_{P\,max} + I_o \quad (5)$$

where:

I_{L1} is the total leakage current into the diode with only a pulse present.

I_{L2} is the total leakage current into the diode with only a level present.

I_{Lout} is the total leakage out of the diode with both a level and pulse high.

I_{SL} is the safety factor with only a level present.

I_{SP} is the safety factor with only a pulse present.

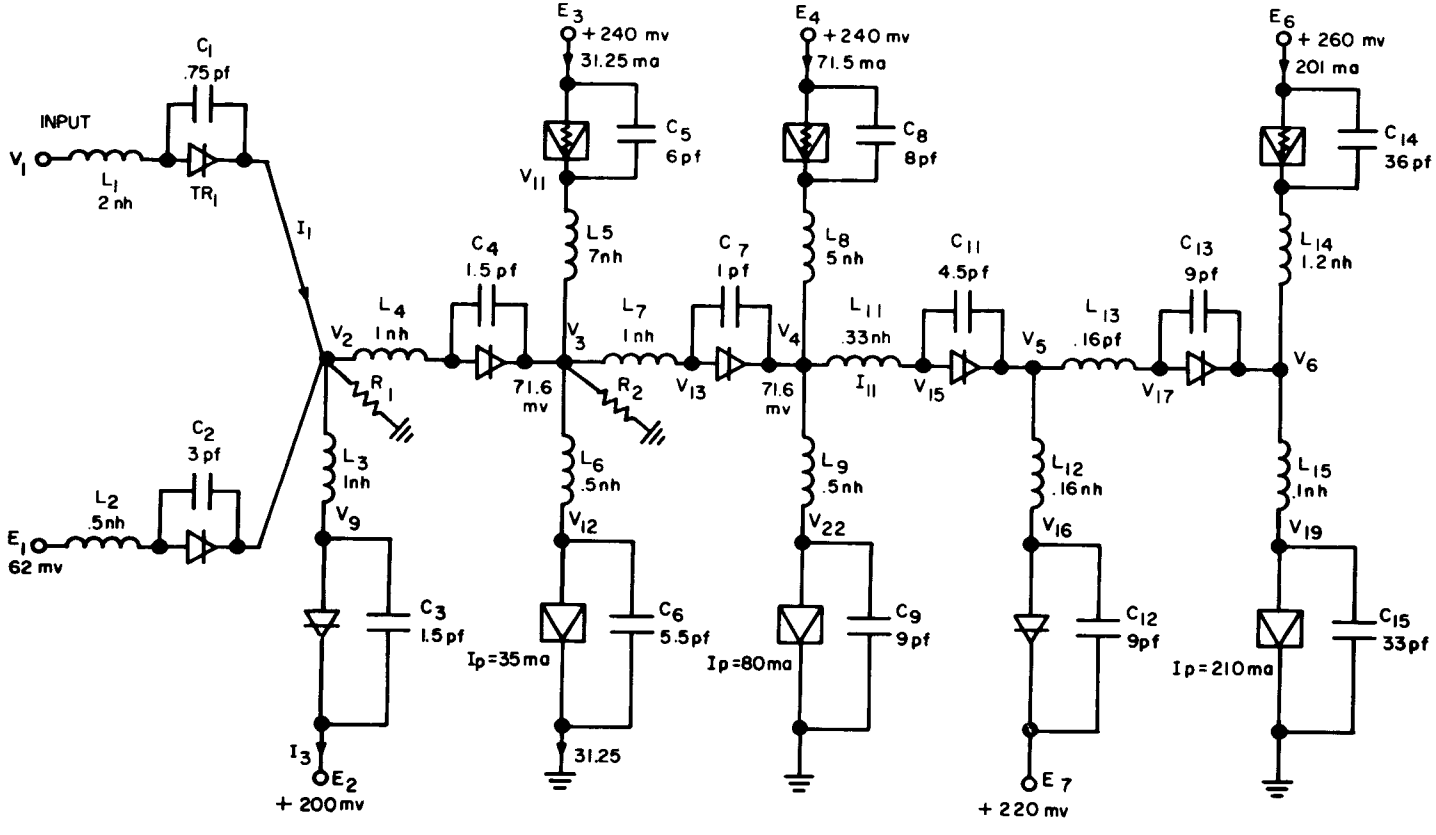


Figure 2-11. Equivalent Circuit of OR Gate Driving Six Other Gates [s]

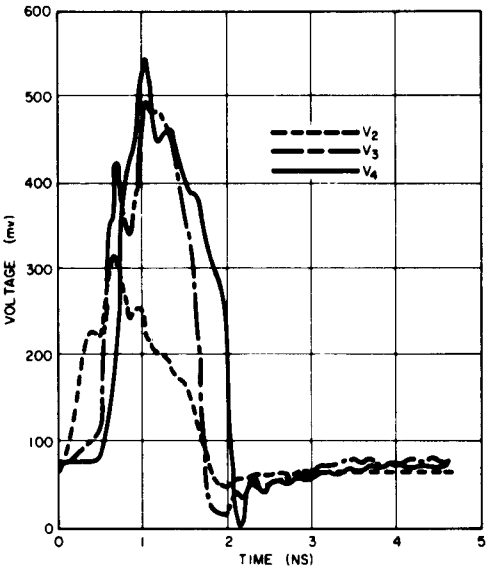


Figure 2-12. Computed Voltage Waveforms for OR Gate of Figure 2-11 [s]

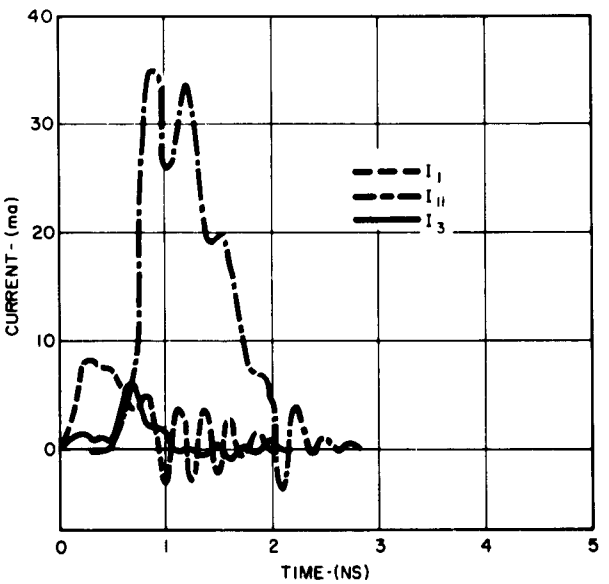


Figure 2-13. Computed Current Waveforms for OR Gate of Figure 2-11 [s]

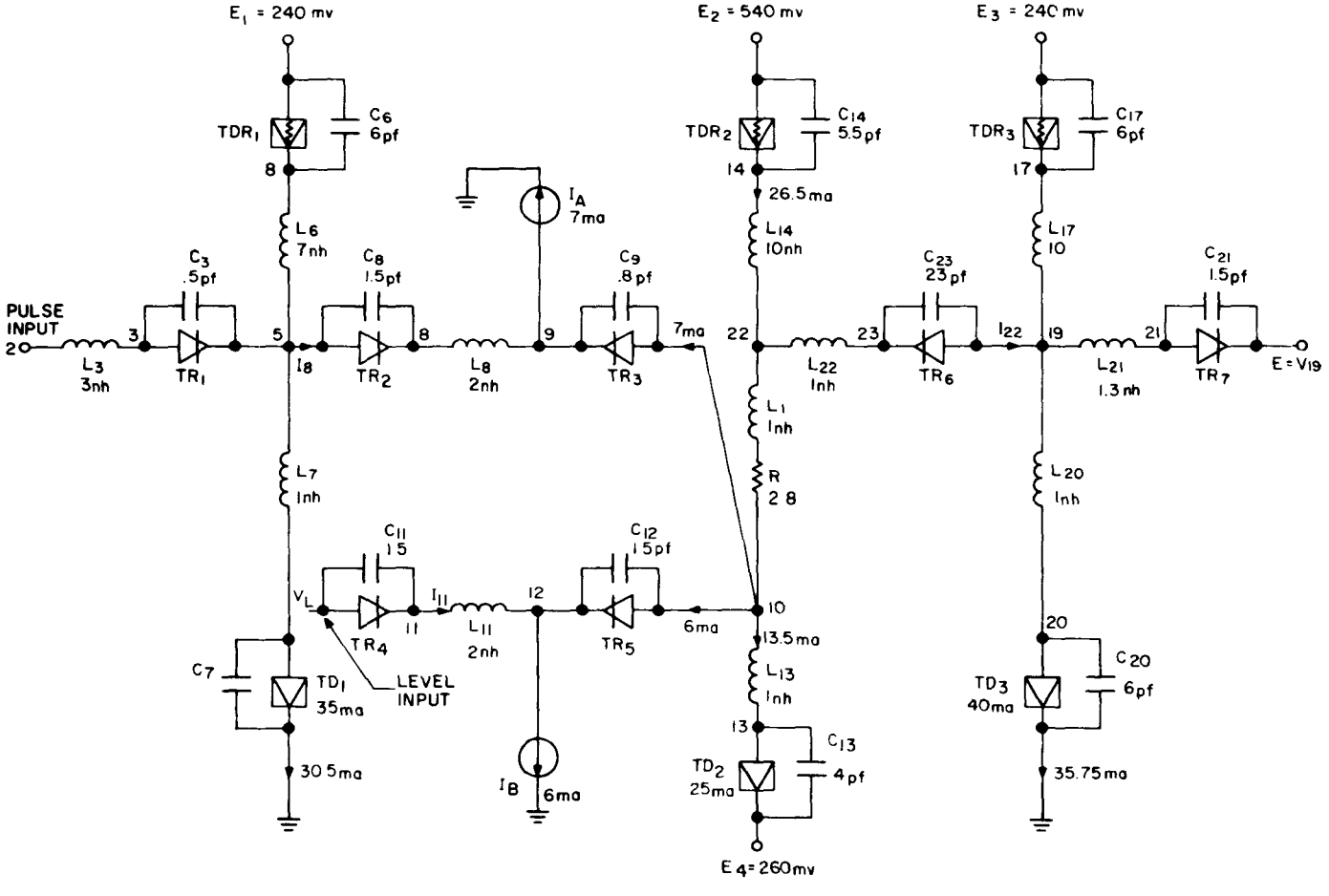


Figure 2-14. Equivalent Circuit of AND Gate [s]

i_L is the nominal level current

i_P is the nominal pulse current

The definitions of I_B, I_o, I_P are the same as those for the OR gate.

The design of the AND gate output stage is the same as that for OR gate which is governed by equations (1) and (2).

Some of the significant calculated values for the AND stage and output stage are given in Table 2-4 below:

TABLE 2-4
CALCULATED CURRENTS FOR AND GATE

Parameter Symbol	AND Stage	Parameter Symbol	Output Stage
I_P	25 ma	I_P	40 ma
I_{L1}	.2 ma	I_{BP} max	4.25
I_{L2}	.5 ma	I_{BP} min = I_S	2.0 ma*
I_o	1.75 ma		
I_{out}	.1 ma	I_{Lin}	.36 ma
I_{SL}	2.7 ma	I_{Lout}	.09 ma
I_{SP}	1.51 ma	I_O	2 ma
i_L	6.0 ma	i_{in}	6.25 ma
i_P	7.0 ma		

* The safety factor for this stage is large enough to tolerate the capacitive feedthrough from 2 of its outputs.

Some of the significant voltage variations without inputs or outputs are:

V_6 = 64 mv to 79 mv

V_{19} = 65 mv to 81 mv (symbols are defined in Figure 2-7)

The circuit model used to study the dynamic behavior of this gate is shown in Figure 2-14. TR_1 approximates the input characteristic of this gate in series with the output TR of the preceding gate. TR_7 represents the series combination of the output TR of this gate with the input characteristic of the following gate. Some of the significant voltage and current waveforms of this gate are shown in Figures 2-15 and 2-16.

c. Bistable Circuit

The set amplifier of the bistable circuit is identical to the first stage of the OR gate. Consequently the same design considerations apply.

The inverter driver is designed in accordance with equations (1) and (2).

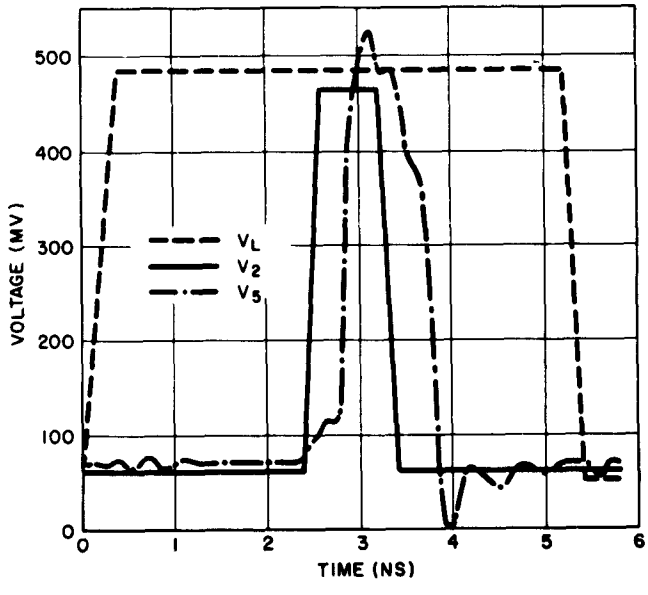


Figure 2-15. Computed Voltage Waveforms for AND Gate of Figure 2-14 [8]

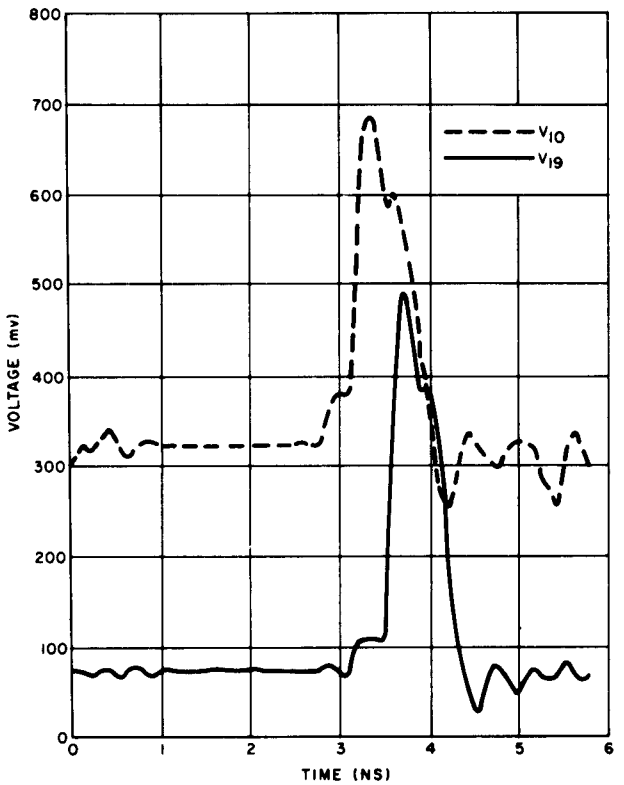


Figure 2-16. Computed Current Waveforms for AND Gate of Figure 2-14 [8]

The inverter is designed in accordance with equations (6) and (7) shown below:

$$I_{B3\ max} \leq I_{P3\ min} - I_{S3} - I_{L3\ in} + I_{B2\ min} \quad (6)$$

$$i_{in3\ min} \geq I_{P3\ max} - I_{B3\ min} + I_{B2\ max} + I_{03} + I_{L3\ out} \quad (7)$$

Definition of symbols is the same as for the OR gate except that the "2" subscripts refer to the inverter driver while the "3" subscripts refer to the inverter.

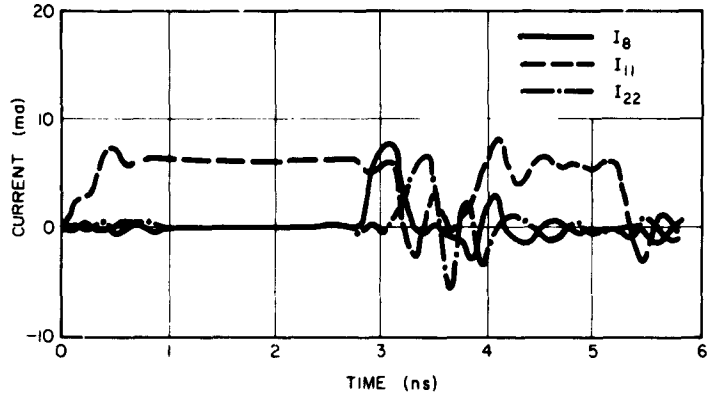


Figure 2-17. Computed Current Waveforms for AND Gate of Figure 2-14 [5]

Some of the significant calculated values for the inverter driver and inverter are given in Table 2-5 below:

TABLE 2-5
CALCULATED CURRENTS FOR INVERTER DRIVER AND INVERTER

Parameter Symbol	Inverter Driver	Inverter
I_P	25 ma	35 ma
$I_{BP\ max}$	3.4 ma	10 ma
$I_{BP\ min} = I_S$	1.5 ma	1.5 ma
I_{Lin}	.3 ma	0
I_{Lout}	1.0 ma	1.0 ma
I_0	1.25 ma	1.75 ma
i_{in}	5.65 ma	11.75 ma

Some of the significant voltage variations without inputs or outputs are:

V_2 = 44 mv to 74 mv

V_6 = -20 mv to -1 mv (symbols are defined in Figure 2-9)

The bistable unit was designed to have a safety factor of 1.2 ma from the valley and 5 ma from the peak. Due to the mode in which the bistable circuit operates, it is difficult to give an accurate analytical expression of the set and reset requirements. Thus, these requirements were determined with a digital computer based on the dynamic operation. The model for studying the set action of the bistable circuit is shown in Figure 2-18; corresponding calculated waveforms are shown in Figures 2-19 and 2-20. The model for studying the reset action is shown in Figure 2-21 with corresponding waveforms shown in Figures 2-22 and 2-23.

Here again TR_1 represents the series combination of the output rectifier from the preceding stage and the input rectifier to this stage. TR_5 and TR_6 in Figure 2-18 represent a worst-case condition for setting the bistable. In Figure 2-21, TR_5 is replaced with R_5 which represents the transmission line. This simulates a worst-case condition for resetting.

Some of the significant static bistable voltage variations are:

V_{13} (low state) = 50 mv to 113 mv

V_{13} (high state) = 472 mv to 510 mv

4. Circuit Interconnections

All interconnections are made with 50-ohm miniature coaxial transmission lines for monostable circuits and 31.5-ohm lines for bistable to AND gate connections. The choice of 50-ohm lines for monostable circuits was based on obtaining optimum coupling efficiently between gates. In some cases the transmission line provides a current amplification of about 1.2. This was taken advantage of whenever possible. The choice of 31.5-ohm lines for bistable circuit coupling was based on a compromise between speed of level build up and operation reliability. For lines with $Z_o > 31.5$ ohms, the build up of the required level is delayed for one or several reflection between the bistable output and the AND gate input. For a $Z_o < 31.5$ ohms, the amplitude of the level increases such that the bistable circuit could operate monostably.

5. Trimming Network Design

a. General

The determination of the initial current supplied to a stage by the trimming network is a compromise between the tolerance of the components specified

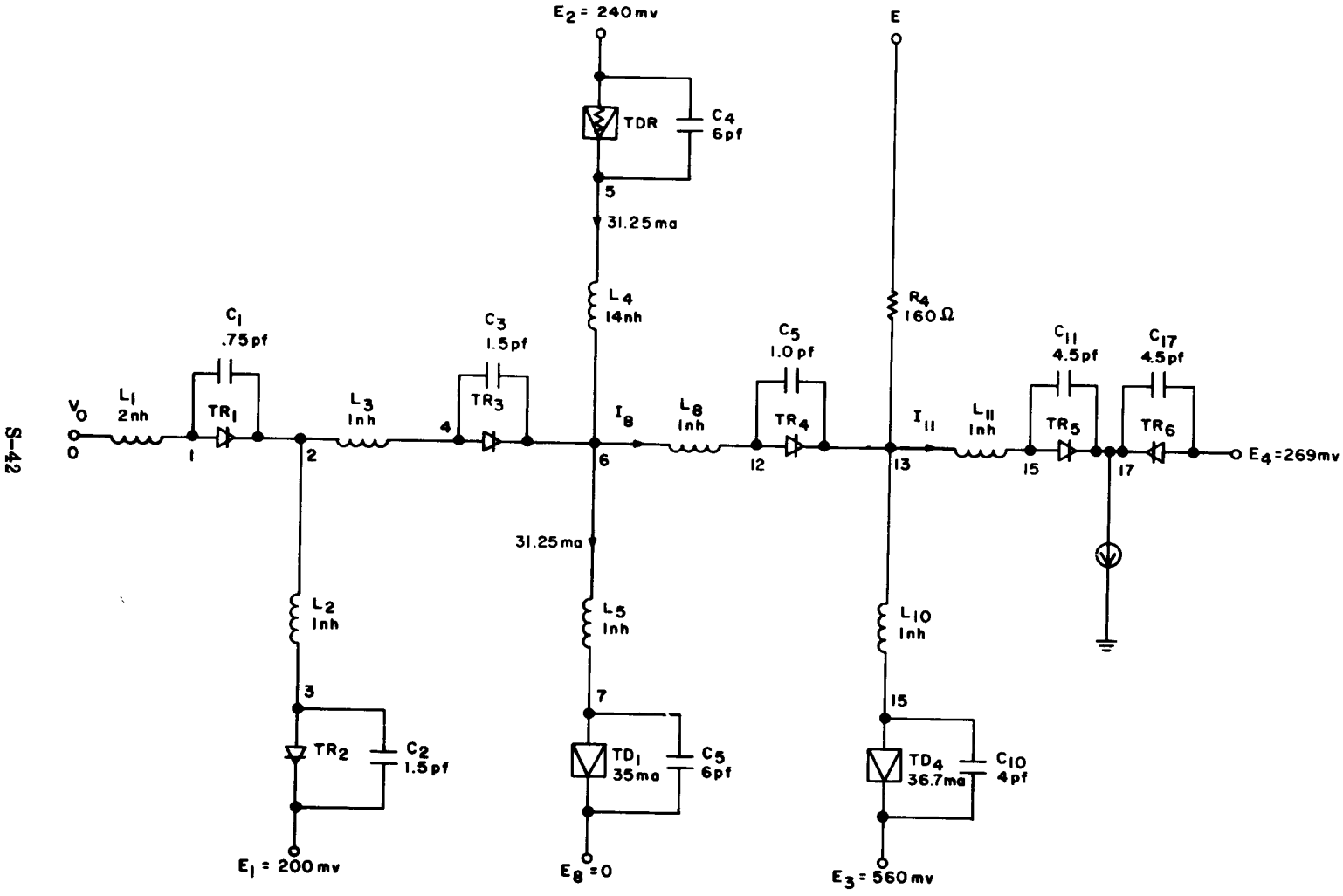


Figure 2-18. Equivalent Circuit of Bistable Setting (s)

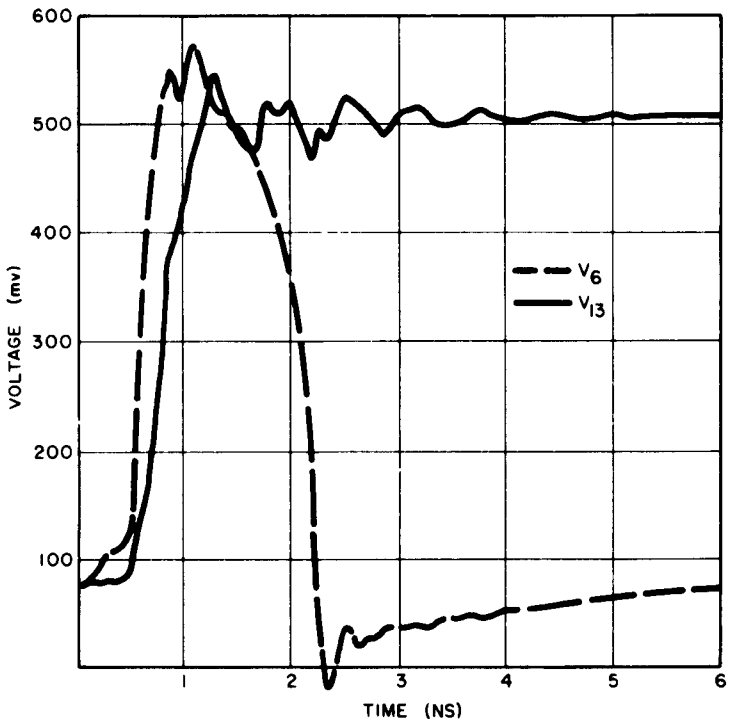


Figure 2-19. Computed Voltage Waveforms for Circuit of Figure 2-18 [s]

for the stage and the total power dissipation of the stage. As the initial tolerances for the tunnel diode and tunnel resistor of the stage are increased, a greater trimming current range is required. This higher trimming current increases the stage dissipation. In this design, an initial tunnel diode peak current and tunnel resistor mid-current tolerance of ±1.5% was selected. It was assumed that resistors could be trimmed up to a two to one range in resistance value. The desired increment of current below the peak after trimming was chosen for each stage to correspond to the worst-case designs for the circuits as determined in paragraph 3. (Design Considerations). This current is the difference between the nominal peak current of the tunnel diode and the nominal bias current of the stage.

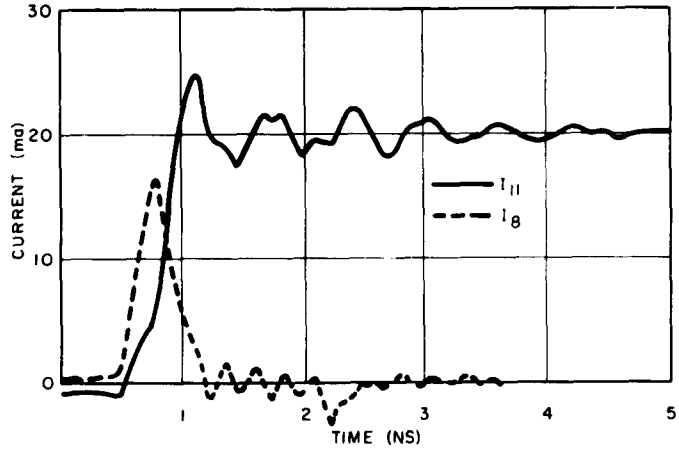


Figure 2-20. Computed Current Waveforms for Circuit of Figure 2-18 [8]

b. OR Gate

The circuit of the OR gate analysed is shown in Figure 2-24. Figure 2-25 is of the first stage and shows the parameters involved in this analysis. These parameters are:

(1) I_T — the trimming current assumed to vary over a 2 to 1 range from $2I_{T\,min}$ to $I_{T\,min}$. This variation in current is accomplished by trimming R_1.

(2) TDR_3 — a tunnel resistor exhibiting a constant-current region over part of its V-I characteristic. The spread of the constant-current region has a minimum band of 50 mv and a typical band of 70 mv, with the mid-voltage varying from about 165 mv for low current units to about 190 mv for higher current units.

(3) TR_1 and TR_3 — identifying numbers for particular tunnel rectifiers.

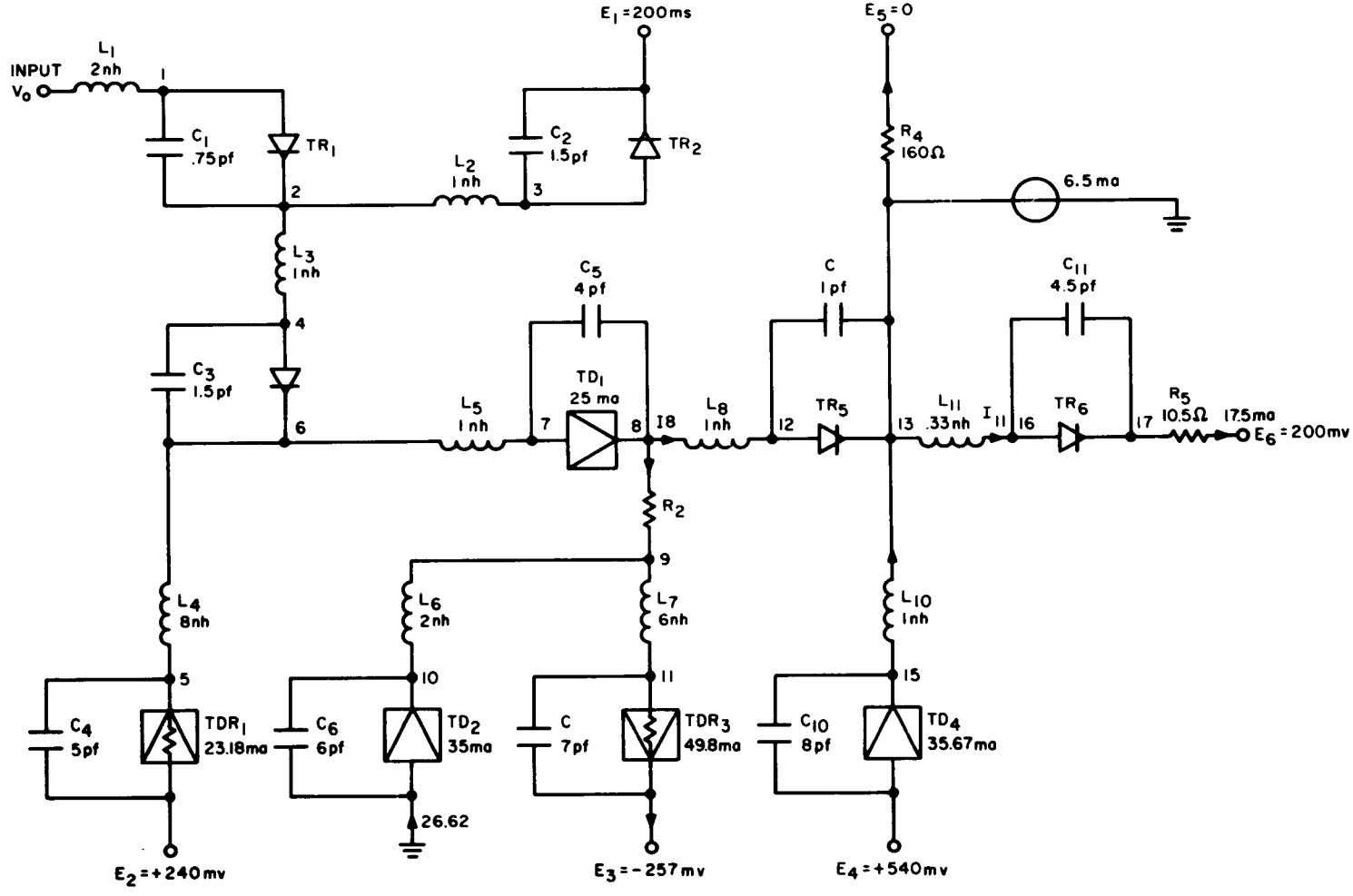


Figure 2-21. Equivalent Circuit of Bistable Resetting [s]

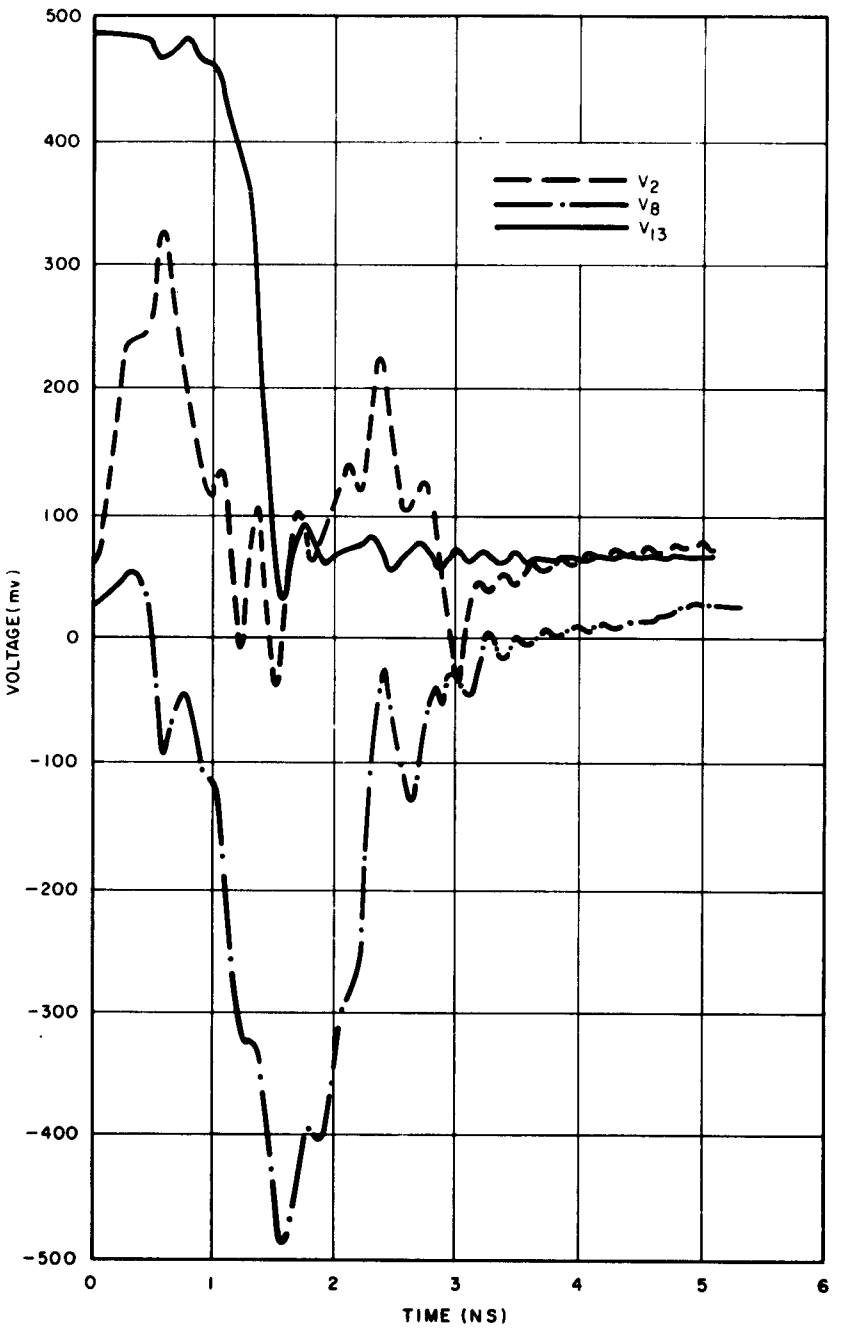


Figure 2-22. Computed Voltage Waveforms for Circuit of Figure 2-21 [8]

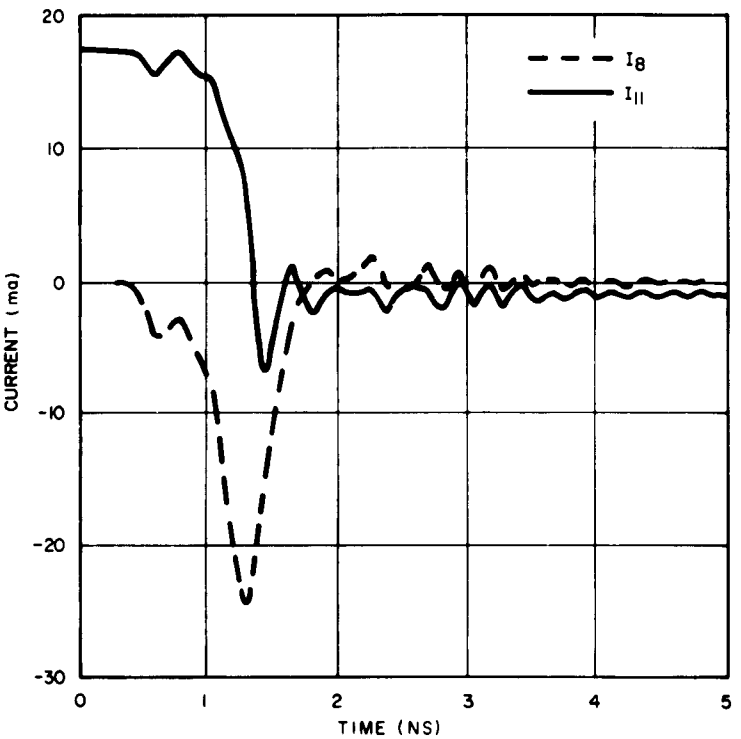


Figure 2-23. Computed Current Waveforms for Circuit of Figure 2-21 [s]

(4) I_{L1} and I_{L2} — static leakage currents which flow through the coupling diodes. One or both coupling diodes may be either forward or reverse-biased depending upon the magnitude and spread of the voltages at nodes V, V_1, V_2, V_3 and + 210 mv. Nodes V_1 and V_2 are the high side of a tunnel diode. I_{L1} and I_{L2} can flow either "in" or "out" of the branch and can be lumped together. The leakage currents flowing toward V can be lumped together and called I_{Lin}. The leakage currents flowing away from V can also be lumped together and called I_{Lout}. Therefore, two possible net leakages exist, one of which can flow into V and the other away from V.

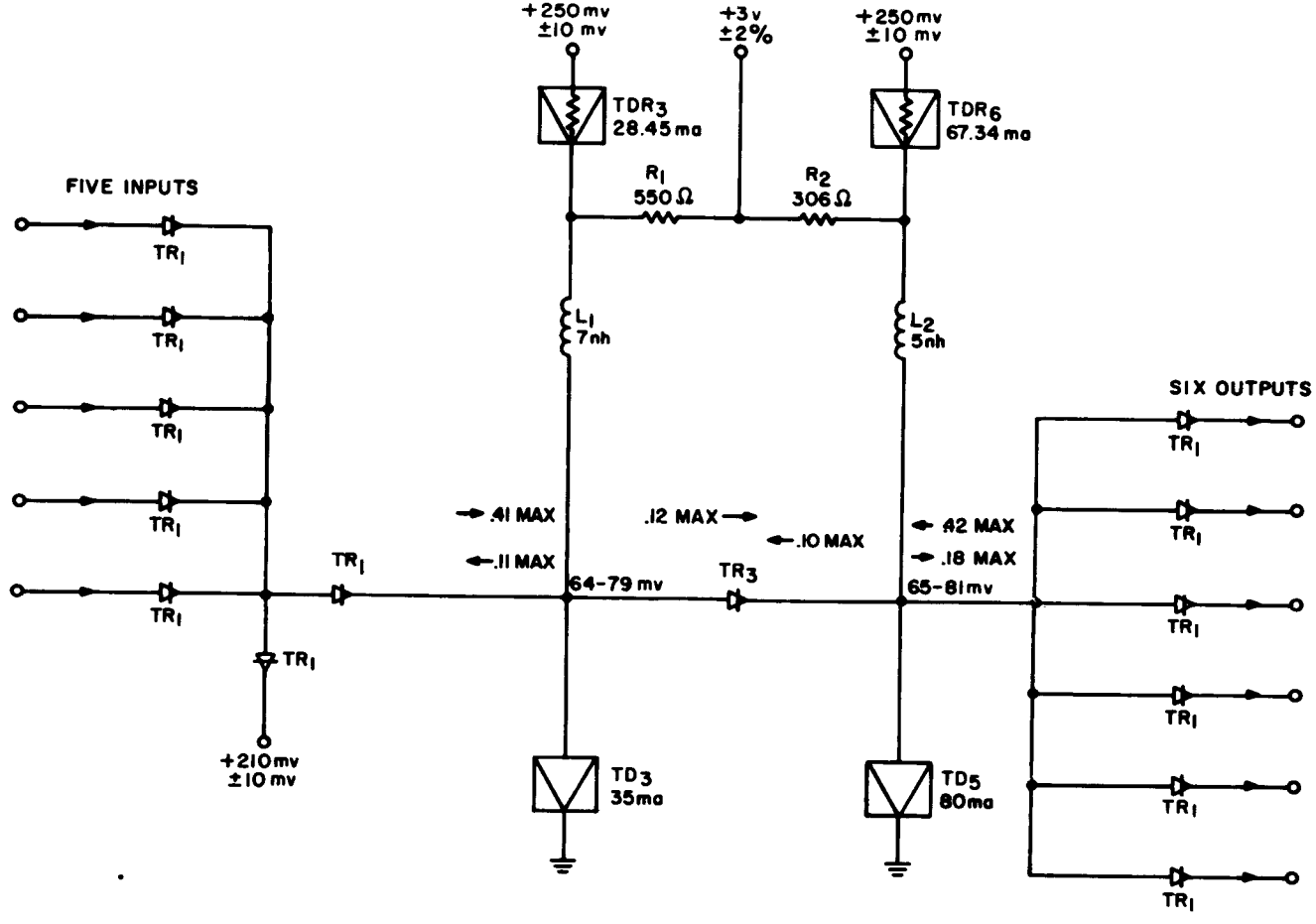


Figure 2-24. OR Gate for 40-Gate Subsystem (s)

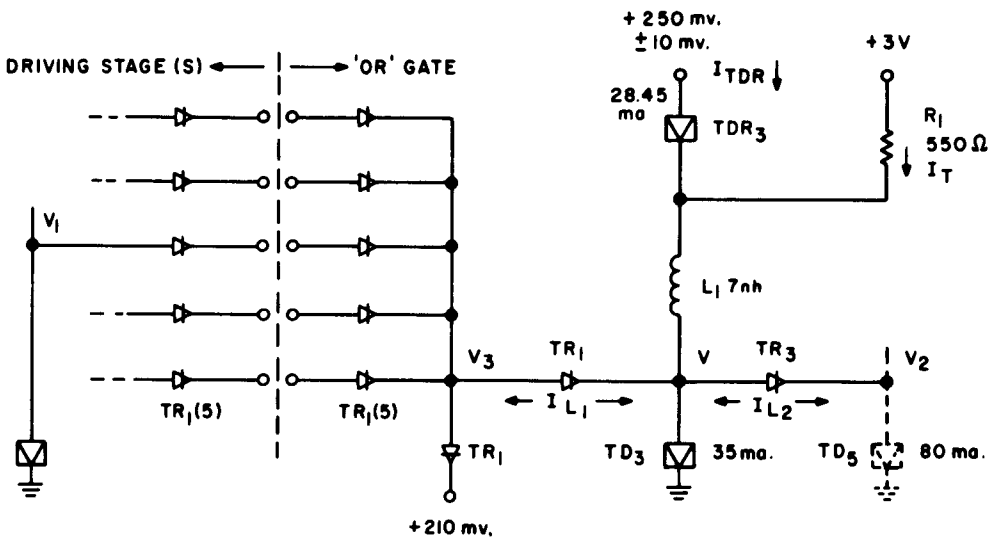


Figure 2-25. First Stage of OR Gate [s]

Current Equations for First Stage of OR Gate

Referring to Figure 2-25, current equations for the circuit are formulated as follows:

$$\underline{I_T} + \overline{I_{TDR}} + I_{Lin} = \underline{I_p} - I_x \quad (1)$$

$$\overline{I_T} + \underline{I_{TDR}} + I_{Lout} = \overline{I_p} - I_x \quad (2)$$

Here, a bar above the parameter denotes a maximum value while a bar below denotes a minimum value. The symbol, I_x, denotes the desired distance below

the peak of the tunnel diode immediately after trimming the circuit. The basic philosophy used in deriving equations (1) and (2) is that the minimum trimming current is required when all other currents entering node V are maximum and the currents leaving node V are minimum. The parameters are defined as follows:

I_p = Nominal tunnel diode peak current.

$\overline{I_p} = I_p(1+A)$. A = tolerance on peak current of tunnel diode. A = .01.

$\underline{I_p} = I_p(1-A)$.

I_{TDR} = Nominal value of tunnel resistor in "flat region".

$\overline{I_{TDR}} = I_{TDR}(1+B)$. B = tolerance on tunnel resistor "constant current". current" region. B = .015.

$\underline{I_{TDR}} = I_{TDR}(1-B)$.

$\underline{I_T}$ = Minimum trimming current.

$\overline{I_T}$ = Maximum trimming current = $2\underline{I_T}$.

I_x = Desired increment of current below the peak just after trimming.

I_{Lin} = Static leakage current into node V.

I_{Lout} = Static leakage current out of node V.

Simultaneous Solution of Current Equations to Yield Equations for the Trimming Current and the Tunnel Resistor

$$\underline{I_T} + \overline{I_{TDR}} + I_{Lin} = \underline{I_p} - I_x \tag{1}$$

$$\overline{I_T} + \underline{I_{TDR}} - I_{Lout} = \overline{I_p} - I_x \tag{2}$$

From (1)

$$\underline{I_T} = I_P(1-A) - I_x - I_{Lin} - I_{TDR}(1+B) \tag{3}$$

Substituting (3) into (2) -

$$2\left[I_p(1-A) - I_x - I_{Lin} - I_{TDR}(1+B)\right] + I_{TDR}(1-B) - I_{Lout} = I_p(1+A) - I_x \tag{4}$$

$$2I_p(1-A) - 2I_x - 2I_{Lin} - 2I_{TDR}(1+B) + I_{TDR}(1-B) - I_{Lout} - I_p(1+A) + I_x = 0$$

$$I_p - 3I_p A - I_x - 2I_{Lin} - I_{Lout} - I_{TDR} - 3I_{TDR} B = 0$$

$$I_p(1-3A) - I_x - 2I_{Lin} - I_{Lout} - I_{TDR}(1+3B) = 0$$

$$I_{TDR} = \frac{I_p(1-3A) - I_x - 2I_{Lin} - I_{Lout}}{1+3B} \qquad (5)$$

Equation (5) can be used to determine the tunnel resistor required for the circuit, assuming the leakage currents are known. With the tunnel resistor known, $\overline{I_{TDR}}$ and $I_{\underline{TDR}}$ can be found and either equations (1) or (2) can be used to find $\overline{I_T}$, the initial trimming current required.

Determination of Leakage Currents

The leakage current flowing through TR_1, I_{L1}, is determined by graphical solution. The solution is affected by a consideration of the voltages at TD_3, the output tunnel diode of the previous driving stage and the +210 mv supply. In addition, the characteristic curve of TR_1 is required. The input circuit to the OR gate is shown in Figure 2-26, V_1 is the central node of the output stage of the previous gate. V is the central node of the first stage of the OR gate which is the high side of TD_3. The variation of the voltages at V_1 and V is known from the worst-case V-I curves for the particular tunnel diodes and the accompanying tunnel resistors and trimming currents. By assuming various values for V_3 and making $I_1 + I_2 + I_3 = 0$, the leakage currents in the various branches are determined. By this method the maximum and minimum values of I_2 can be computed, I_2 being the leakage current I_{L1}. This leakage current turns out to be 0.41 ma into TD_3 and 0.11 ma out of TD_3. The leakage current can vary between these two limits. With the leakage currents known the tunnel resistor and trimming current can be determined. The desired current below the peak for this stage is 2.45 ma. The tunnel resistor required for the first stage is nominally 28.45 ma and the initial trimming current is 5.36 ma. The spread of the voltage at TD_3 is 64 to 79 mv.

Second Stage of OR Gate

The second stage of the OR gate is treated exactly the same as the first stage. Leakage currents for this stage turn out to be 0.42 ma into TD_5 and 0.18 ma out of TD_5. Leakage currents through the coupling diode, TR_3, are 0.12 ma in the forward direction and 0.1 ma in the back direction. The voltage range across TD_5 is 65 - 81 mv. The tunnel resistor current for this stage is 67.34 ma and the initial trimming current is 9.6 ma. The desired current below the peak for this stage is 5.3 ma. This consists of the safety current, aging considerations of the tunnel resistor and tunnel diode peak currents, and a current factor to account for bias supply voltage variations. Under worst-case conditions the tunnel diode will not be biased closer to the peak than by the margin of the safety current. Aging of the tunnel diode peak current is assumed to be +1% of I_p. Aging of the tunnel resistor is also assumed to be +1%. A change of +1% in the tunnel diode bias current is caused by power supply voltage variations stemming from power supply tolerances. Leakage currents and stage voltages for the OR gate are shown in Figure 2-24.

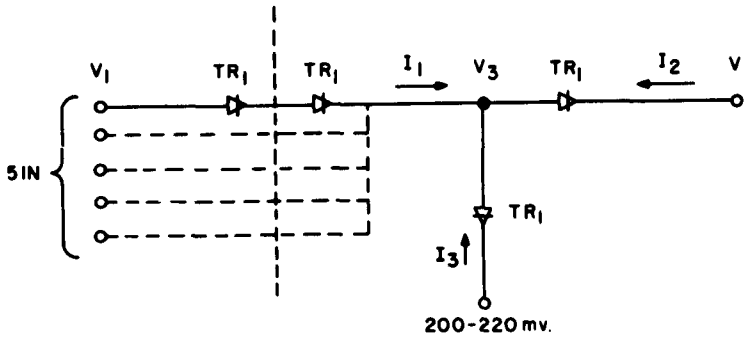


Figure 2-26. Input Circuit to OR Gate [5]

c. AND Gate

(1) Pulse Buffer Stage

The first stage of the AND gate (Figure 2-27), the pulse buffer stage, is similar to the first stage of the OR gate and thus is treated in the same manner. In fact, the two stages are identical except for the output coupling diode which alters the leakage current slightly in this branch of the circuit. The fundamental equations for the tunnel resistor and trimming current as used for the OR gate are also used to specify these parameters for the pulse buffer stage. The leakage current into TD_3 can be as much as 0.91 ma, and 0.11 ma out of TD_3. The leakage currents were determined in the same way as for the OR gate. The voltage range across the tunnel diode is approximately 64 - 79 mv. The tunnel resistor required for this circuit is expressed as:

$$TR = \frac{I_p (1-3A) - (1) - 2L_{in} - L_{out}}{1 + 3B}$$

$$= \frac{35(.97) - 2.45 - 2(.91) - .11}{1.045}$$

$$= \frac{33.95 - 2.45 - 1.82 - .11}{1.045}$$

$$= 28.25 \text{ ma}$$

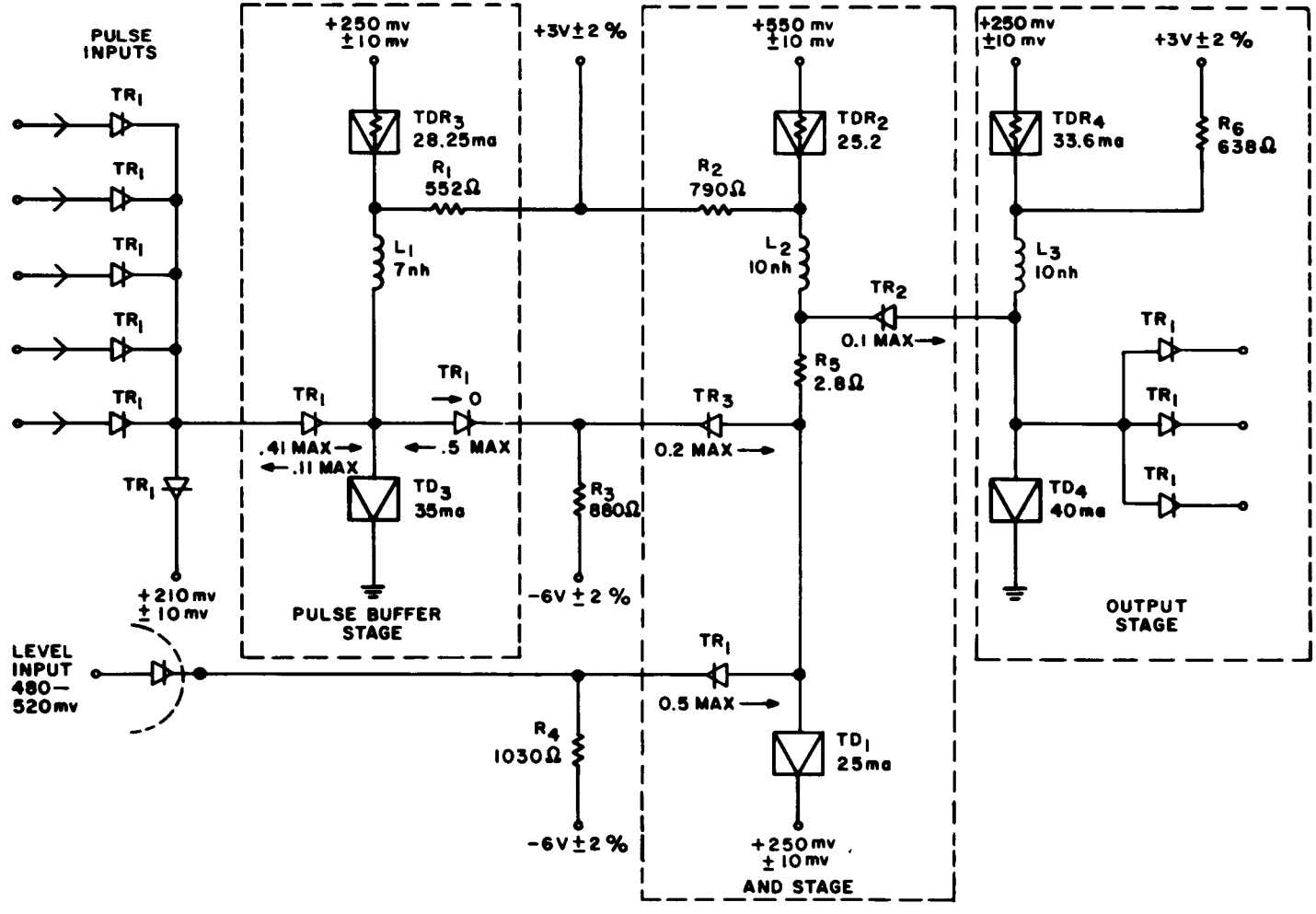


Figure 2-27. AND Gate for 40-Gate Subsystem [5]

The minimum trimming current (I_T) required is -

$$\underline{I_T} = \underline{I_p} - (1) - L_{in} - \overline{TR}$$

$$= 34.65 - 2.45 - .91 - 28.25\ (1.015)$$

$$= 2.62 \text{ ma.}$$

Initial Trimming Current = $2 \times 2.62 = 5.24$ ma.

Desired Distance Below Peak = $I_{Safety} + 1\%\,TDR + 1\%\,I_p + 1\%\,I_B$

$$= 1.5 + .3 + .35 + .3 = 2.45 \text{ ma.}$$

(2) AND Stage

Operation of AND Stage

A schematic diagram of the AND stage is shown in Figure 2-28. With both a pulse and a level applied to the AND gate, TR_1 adjacent to R_4 and TR_3 adjacent to R_3 are both cut off and the current that had been flowing through them is diverted into TD_1 (the 25-ma diode for the AND stage). R_3 and the -6 volt supply produce a 7-ma current source. Likewise, R_4 and the -6 volt supply produce a 6-ma current source. The leakage currents in TR_3 and TR_1 must be considered when they are cut off. With the pulse input activated, coupling rectifier TR_3 can pass 0.2 ma maximum into the tunnel diode. With the level input high the maximum leakage through TR_1 can be 0.5 ma into the tunnel diode. The smallest leakage current passed by the two input coupling rectifiers can be 0 ma under certain conditions of operation. The output coupling tunnel rectifier, TR_2, is always reverse-biased in the valley region and will conduct a leakage current of about 0.1 ma. There are three modes of operation considered for the AND stage. These are:

(a) Level on; pulse on; gate must fire.

$$\underline{I_B} - \overline{I_{Lout}} \geq \overline{I_p} + I_{OD} \qquad (1)$$

Where I_{OD} is the current overdrive for the tunnel diode = $7\%\ I_p$.

$I_p = 25$ ma $\qquad \Delta I_p = \pm 1\%\ I_p \qquad \overline{I_{Lout}} = 0.1$ ma.

$\Delta I_B = \pm 3\%\ I_B$; 1% for aging and 2% for bias variation.

From (a) equation (1)

$$\underline{I_B} = 25.25 + 1.75 + 0.1 = 27.1$$

$I_B = 27.9$ ma

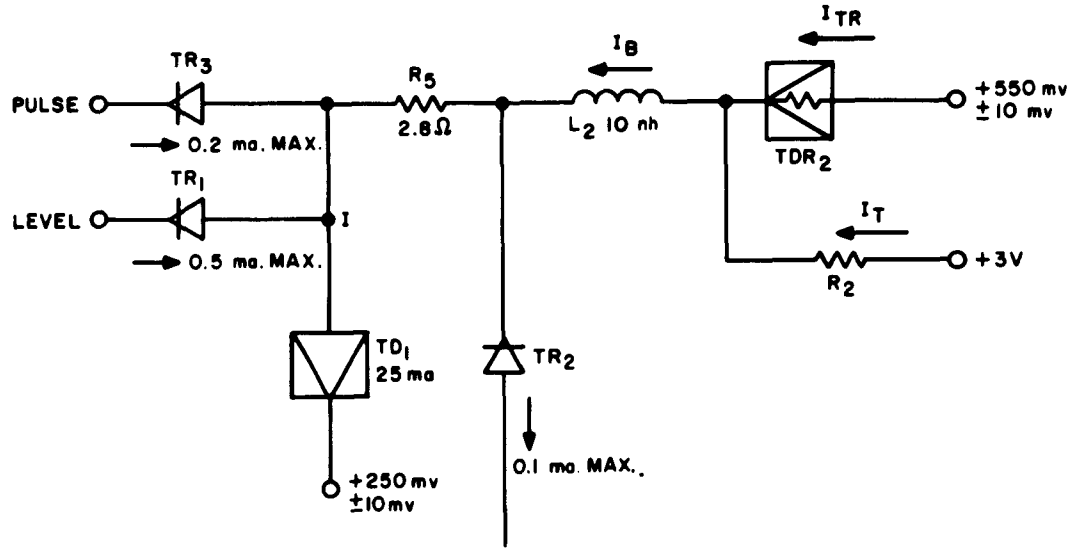


Figure 2-28. AND Stage [5]

$\underline{I_B}$ = 28.8 ma, assuming I_B is trimmed initially to be 2.9 ma above initial I_p. The 2.9 ma is a factor composed of the overdrive current, aging of the tunnel diode and tunnel resistor and bias supply variations.

(b) Level off; pulse on; gate must not switch.

$$\overline{I_B} + \overline{I_{Lin}} - \underline{I_L} \leq \underline{I_p} - I_{SAFETY} \qquad I_L = 6.0 \text{ ma} \pm 4\%$$

$$I_{SAFETY} = 24.75 + 5.82 - 0.2 - 28.8$$

$$= 1.51 \text{ ma (Pulse ON)}$$

(c) Level on; pulse off; gate must not fire.

$$\overline{I_B} + \overline{I_{Lin}} - \underline{ip} \leq \underline{I_p} - I_{SAFETY} \qquad ip = 7.0 \text{ ma} \pm 4\%$$

$$I_{SAFETY} = 24.75 + 6.8 - 0.5 - 28.8$$

$$= 2.17 \text{ ma (Level ON)}$$

AND Stage Trim Current Calculations

$$I_B = I_{TR} + I_{TRIM} \qquad (2)$$

$$\underline{I_B} = \overline{I_p} + I_{OD} + \overline{I_{Lout}} \qquad \text{(aging and bias tolerances)}$$

$$0.97 I_B = 1.01 I_p + 1.75 + 0.1$$

$$I_B = 1.04 I_p + 1.91$$

If the peak current varies by ±1% due to initial tolerance, and the tunnel resistor varies by ± 1.5% and the trim current varies over a 2 to 1 range, then from equation (2) -

$$\overline{I_{TR}} + \underline{I_{TRIM}} = \underline{I_B}$$

$$\underline{I_{TR}} + \overline{I_{TRIM}} = \overline{I_B}$$

$$1.015 I_{TR} + 0.5 I_{TRIM} = (1.04 I_p) .99 + 1.91 \text{ ma}$$

$$.985 I_{TR} + I_{TRIM} = (1.04 I_p) 1.01 + 1.91 \text{ ma}$$

For $I_p = 25$ ma

$$1.015 I_{TR} + 0.5 I_{TRIM} = 27.7$$

$$.985 I_{TR} + I_{TRIM} = 28.1$$

Substituting from above -

$$1.015 I_{TR} + .5(28.1 - .985 I_{TR}) = 27.7$$

$$.523 I_{TR} = 13.6$$

$$I_{TR} = 26 \text{ ma}$$

$$I_{TRIM} = 28.1 - 25.6 = 2.5 \text{ ma}$$

Present design calls for a 25.2 ma tunnel resistor for this stage. This value was determined for a slightly different circuit configuration than now exists. The circuit was altered slightly to improve performance. It is felt that this stage will operate satisfactorily since the change in the tunnel resistor and trimming current is small. The values given above are to be construed as proper for the present circuit configuration. The parameters were not changed since the former values had already been specified and tunnel resistors ordered.

If TR = 25.2 ma

I_{TRIM} = 28.1-.985 (25.2) = 28.1 -24.8 = 3.3 ma

XI_{TRIM} = 27.7 -1.015 (25.2) = 27.7 -25.6 = 2.1 ma

$$X = \frac{2.1}{3.3} = 0.64$$

which is acceptable.

$$R_{TRIM} = \frac{3-0.4}{3.3 \text{ ma}} = \frac{2.6V}{3.3 \text{ ma}} = 790 \text{ ohms}$$

The 6- and 7-ma current sources have tolerances of ±4%. Two percent is for power supply tolerance, one percent is for initial tolerance of current source resistor and one percent is for aging of the resistor.

(3) Output Stage

The output stage is straightforward. The tunnel diode for this stage, TD_4, is returned to ground which makes the circuit easier to treat. The fundamental equations as derived from the OR gate can be utilized here also. The desired distance below the peak is -

$$(1) = I_{SAFETY} + I_{P_{aging}} + I_{TDR_{aging}} + \text{TDR Bias Variation.}$$

(1) = 1.5 + .4 + .35 + .35 = 2.6 ma

The tunnel resistor required for this stage is expressed as -

$$TR = \frac{I_p (1-3A) - (1) - 2 L_{in} - L_{out}}{1 + 3B}$$

$$= \frac{40(1-.03) - 2.6 - 2(.51) - .1}{1 + .045}$$

= 33.6 ma

The minimum trimming current I_T required is -

$$I_T = I_p - (1) - L_{in} - \overline{TR}$$

= 39.6 - 2.6 - .51 - 33.6 (1.015)

= 2.4 ma

Initial Trim. 1 = 2 x 2.4 = 4.8 ma

Leakage currents were solved for as in previous cases, i.e., by graphical solution.

6. Experimental Results

a. Wafers

Figure 2-30 shows a disassembled wafer as well as a number of assembled wafers. The disassembled wafer has 12 signal connections and 6 power supply connections. The signal connections are on top of the wafer; power is supplied to the back of the wafer. Each power supply connection is shunted by a high-dielectric pad which serves as a capacitance to absorb transients due to circuit switching. In the circuit layout, care was taken whenever possible to keep stray inductances and capacitances to a minimum. In several cases the tunnel diodes had to be mounted in a flat position in order to reduce the stray inductance to a tolerable value. This was especially true with the output stages of the AND gate and OR gate.

Circuits of this kind were constructed and trimmed in accordance with a trimming procedure established for each circuit. The circuits were then tested for electrical performance, which indicated reliable operation and good agreement with theoretical and computed results.

The AND and OR wafers were tested at 300 mc, and the bistable wafer was tested with the set and reset pulses arriving at a 150 mc rate. The worst-case delays on these wafers were:

AND - 1.0 nsec

OR - 0.65 nsec

Set - 0.75 nsec

Reset - 1.0 nsec

Typical output waveforms from these wafers are shown in Figure 2-31 to 2-33.

b. Termination

In order to test the termination network's effectiveness in decreasing reflections, the circuit of Figure 2-34 was tested. The AND gate was driven from a high-impedance source through a 50-ohm cable while observing P_1 for reflections. The reflected voltage seen at P_1 is the open circuit voltage of the reflected pulse. The photograph of Figure 2-35 shows both the driving pulse and reflected pulse for two values of E_B. When E_B was raised to 520 mv, very little termination was provided by the network. When E_B was set at its nominal value of 210 mv, most of the driving pulse was absorbed. The reflected pulse shown has an amplitude of less than 100 mv with E_B set at 210 mv. This means that less than 1 mv of current is reflected from the termination network.

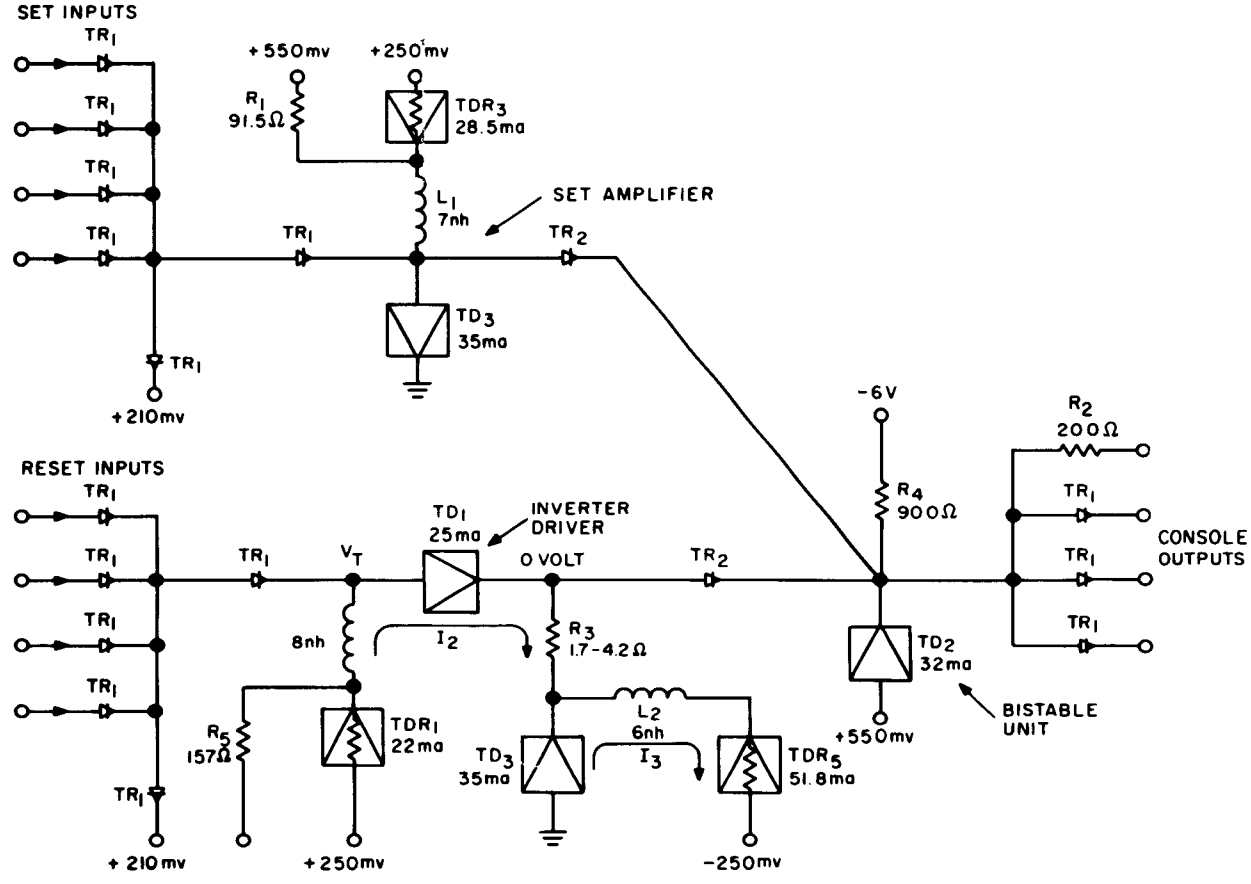


Figure 2-29. Bistable Circuit for 40-Gate Subsystem [s]

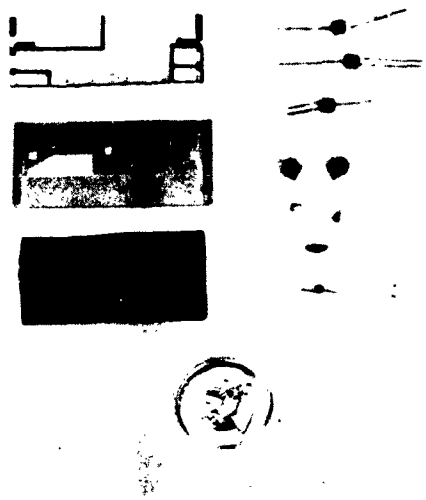


Figure 2-30a. Disassembled Wafer [s]

Figure 2-30b. Assembled Wafers, Front and Back Views [s]

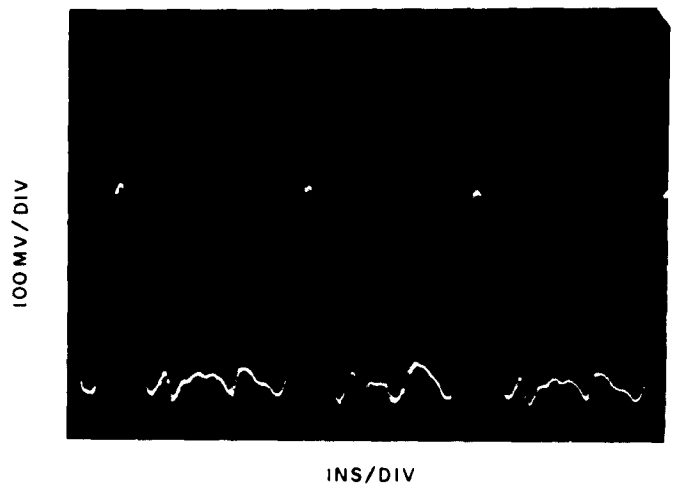


Figure 2-31. OR Gate Output Voltage Waveform [s]

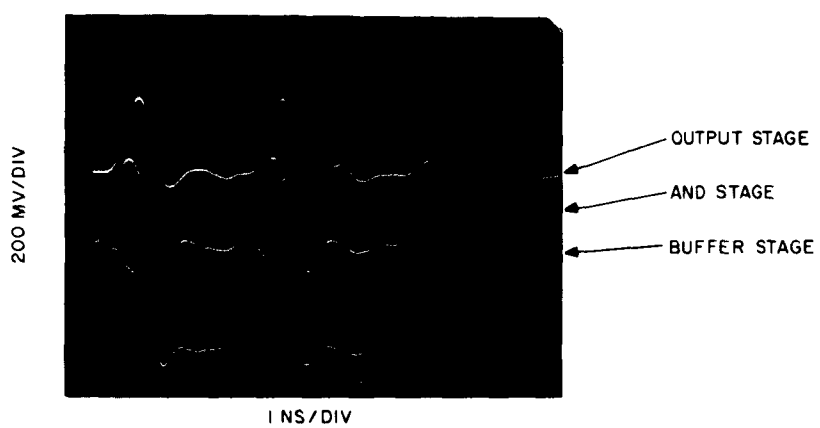


Figure 2-32. AND Gate Voltage Waveforms [s]

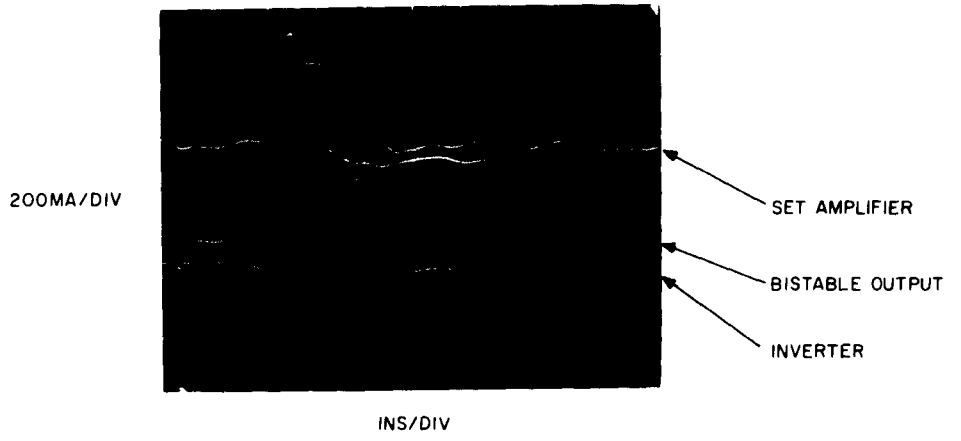


Figure 2-33. Bistable Circuit Voltage Waveforms [5]

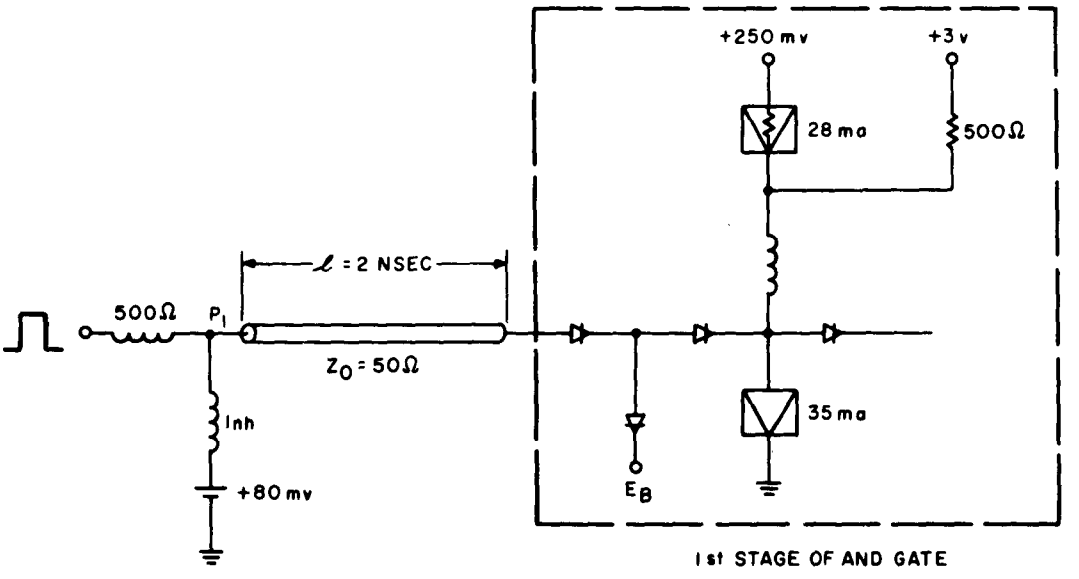


Figure 2-34. Termination Network Test Circuit [5]

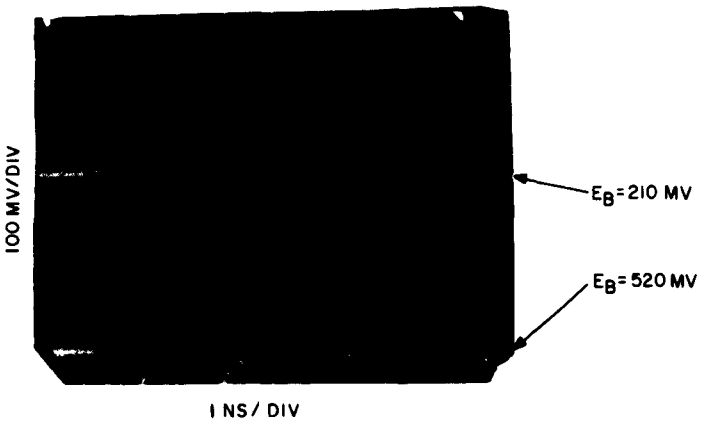


Figure 2-35. Waveform at P_1 of Test Circuit (Figure 2-34) [5]

B. FABRICATION

1. Trimming

Trimming of one resistor per circuit stage is utilized to compensate for the affect of the initial tolerances of the devices on the static bias of a stage. All circuit stages are trimmed except the bistable output stage. In this process, a resistor is abraded to adjust the bias current closely to a known value below the peak current of the tunnel diode in the stage. This trimming resistor, returned to +3 volts in most cases, carries only enough of the total stage bias current to compensate by tolerances. Thus it carries only 20% of the stage current and minimizes dissipation. In this trimming process, the peak current of the tunnel diode itself is used as the threshold to determine the extent of resistor trimming. A 100% increase in resistor value is the maximum trimming capability assumed. The trimming process consists of injecting an accurately measured d-c current into the stage through an input or output rectifier. Also injected through this same terminal is a negative pulse of sufficient amplitude and width to stop the stage from oscillating when its total bias current is slightly greater than the peak current. This pulse is passed through a low-pass filter to insure sufficiently long rise and fall times so that ringing and overshoot are not produced.

Initially, the total current to the stage is greater than the peak and the circuit oscillates. Oscillations are detected on a meter or oscilloscope. As the resistor is trimmed the bias point approaches the peak with the negative input pulse stopping oscillations periodically, enabling precise adjustment to the peak. When the trimming proceeds to the point where the oscillations cease, the total bias current is equal to the peak current of the diode. Removal of the d-c input current assures an initial bias point of the stage a known distance from the peak. During trimming, all power supply voltages, inputs and outputs to the stage are set to a specified level.

A trimming test fixture was set up in the laboratory and 6 wafers were trimmed by this process. Life tests have been conducted on resistors (from 2 sources, ACI and Pyrofilm) trimmed in this fashion. The results of these tests indicate that the resistors must be recoated with a protective material after trimming. A liquid silicone made by Dow Corning is used for this purpose and requires a curing process. Life tests of resistors trimmed, coated and cured show an initial increase in resistance of approximately 1 - 2%. After this initial increase, the resistors are sufficiently stable. This change will be corrected by a second minor trimming which will follow the initial trimming process by a suitable aging period.

2. Trimming and Life Test of Pyrofilm Resistors

A group of eight pyrofilm resistors were soldered onto a wafer, trimmed to twice their original value, recoated, cured and then placed under a life test with approximately 6 volts across each resistor. The test was run for 650 hours (about 27 days). The trimming was done by hand with an abrasive pencil, which is about 3 inches long and tapers down to a fine point. It takes about a minute of abrading to remove the original coating on the resistor; from this point, the resistance can be changed rapidly or slowly depending upon the pressure and length of the pencil strokes. In general, trimming can be accomplished in a few minutes. The resistors were trimmed 100 percent with approximately one-half of the resistive material being removed in the process. By removing this much material the wattage rating is halved. Pyrofilm resistors are rated at about 125 mw and thus after trimming their rating is diminished to 62 mw. After trimming, the resistors were recoated with a viscous, clear, liquid silicone made by Dow-Corning (designated R-6-0031). Following recoating the resistors were cured in an oven at 100°C for 1 hour. After curing the resistors were measured on a Wheatstone Bridge and then placed under a 6-volt life test.

Figure 2-36 is a diagram of the life-test circuit which consists of a series-parallel arrangement of resistors. The value of the trimmed resistor was found indirectly through voltage measurements. Voltages were measured both across the standard resistor, and the trimmed resistor. The value of the trimmed resistor was determined by the relation $R_X = R_S \frac{E_X}{E_S}$. The voltage measurements were made with a John Fluke precision differential DC voltmeter, Model 803.

Figure 2-37 is a graph of resistance change vs. time for five of the test resistors: R_1, R_2, R_5, R_6 and R_7. R_1, R_2 and R_7 were fairly stable throughout the test. R_5 and R_6 were fairly stable after a sharp change during the first 20 hours of life test. R_2 did not show any change at all during test. (Note that zero hours represents a short while after the resistors were placed under load.) The largest resistance change was for R_5, about 0.5%, after the resistor stabilized. It can be seen that as power dissipation in the resistor increases, the resistance changes. R_5 which dissipated 77 mw is somewhat overloaded. Figures 2-38 and 2-39 show that R_3 and R_4 changed about 100% initially but then remained stable for the duration of the life test. After trimming, these resistors dissipated about 112 mw and after stabilizing to twice their trimmed value they dissipated 57 mw. Operating at 112 mw power dissipation, about twice their rated value probably caused the great change in resistance. Figure 2-40 shows the characteristics of R_8 throughout the

$R_1 = 1254\,\Omega$	R_1 STD $= 1057\,\Omega$
$R_2 = 1143\,\Omega$	R_2 STD $= 1020\,\Omega$
$R_3 = 321\,\Omega$	R_3 STD $= 376.4\,\Omega$
$R_4 = 320.8\,\Omega$	R_4 STD $= 378.2\,\Omega$
$R_5 = 468.1\,\Omega$	R_5 STD $= 506\,\Omega$
$R_6 = 2076\,\Omega$	R_6 STD $= 2514\,\Omega$
$R_7 = 2064\,\Omega$	R_7 STD $= 2048\,\Omega$
$R_8 = 2156\,\Omega$	R_8 STD $= 2514\,\Omega$

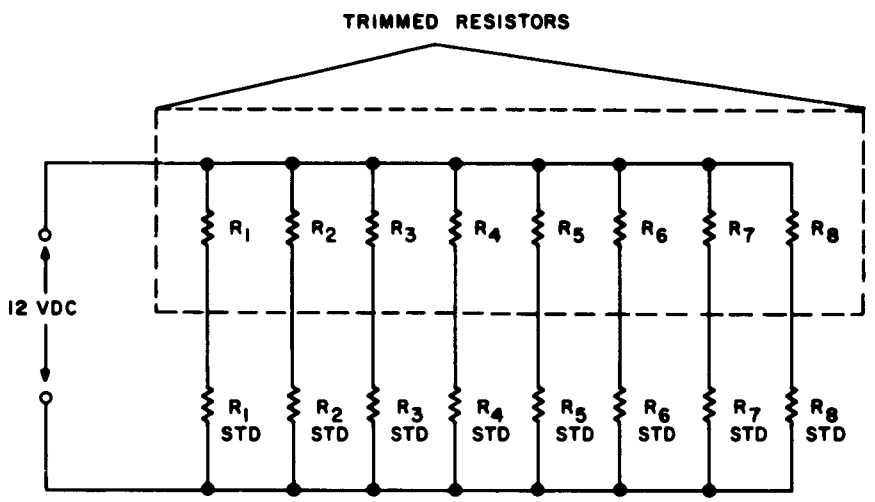


Figure 2-36. Circuit for Resistor Life Test [s]

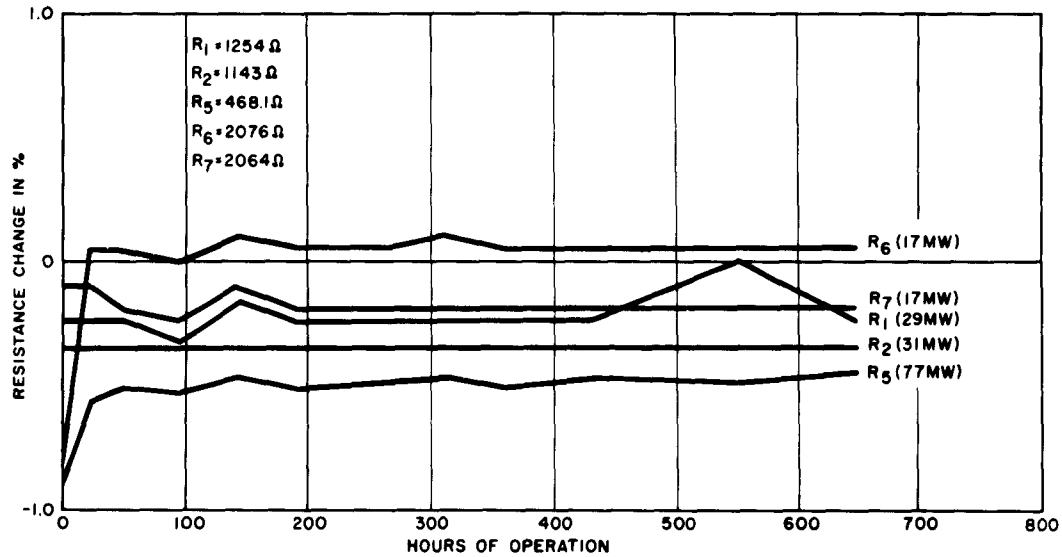


Figure 2-37. Life Test Data of Trimmed Pyrofilm Resistors [s]

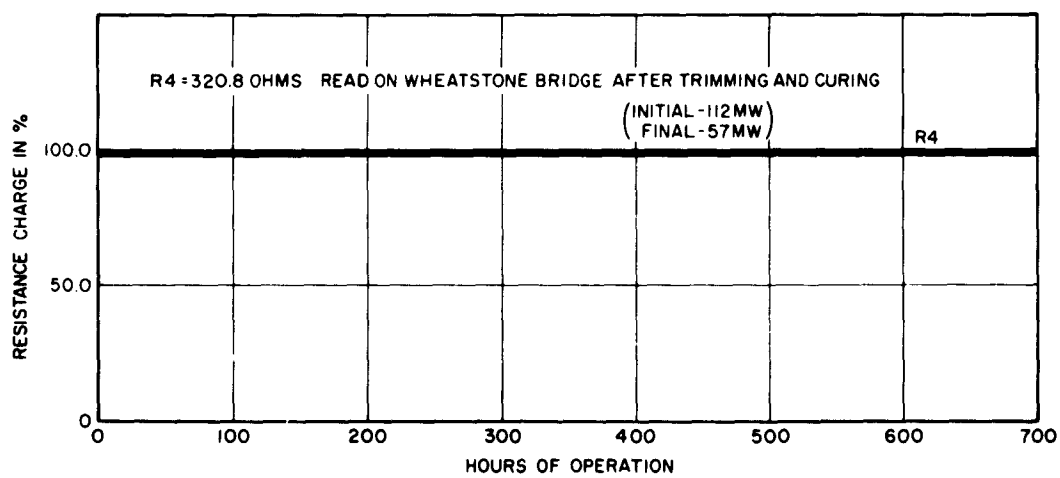


Figure 2-38. Life Test Data of Trimmed Pyrofilm Resistors [s]

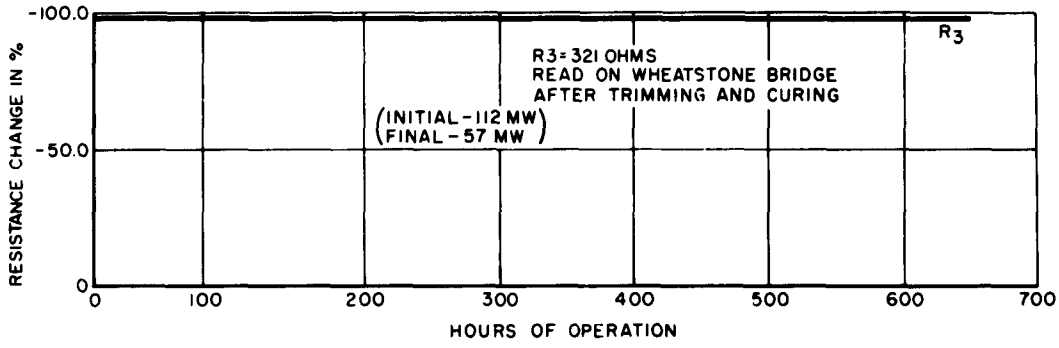


Figure 2-39. Life Test Data of Trimmed Pyrofilm Resistors [s]

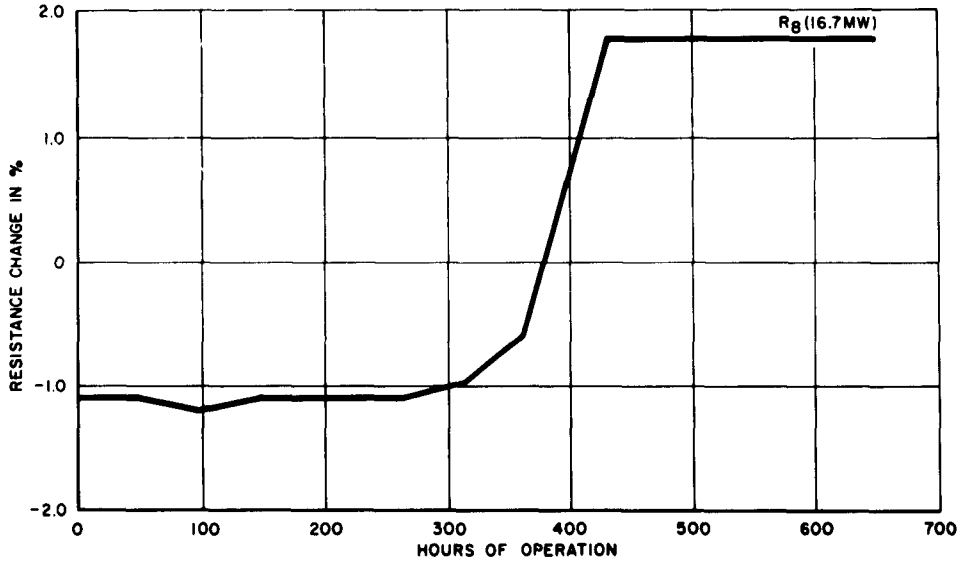


Figure 2-40. Life Test Data of Trimmed Pyrofilm Resistors [s]

life test. Initially, the resistance changed -1.1% and remained at that level for 300 hours. Next it took a large change upwards to +1.8% and remained stable thereafter. This resistor was operated at 17 mw, well below its rated value of power dissipation. No cause can be suggested for this sharp change or subsequent stability. Another test is now under way and it is hoped more light will be shed on the ambiguities.

It was noticed that the trimmed resistors changed value during recoating and curing. The change varied between +0.5% and +3%. Consultation with the manufacturer revealed that they also experienced this trend. They compensate for this in the trimming operation by purposely trimming to a value that is 1% lower than that desired. The manufacturer has noticed a variation of +0.5 to +1.5% after recoating and curing.

Additional life test data is presently being accumulated on a second batch of resistors. Also further tests are being carried out to determine whether stability is a function of the trimming method (does the stability vary if the trimming is done by the air abrasive machine or by hand with an abrasive stone).

3. Trimming of Wafers

The worst-case analysis of the circuits in the 40-gate subsystem accepts trimming of certain resistors in each of the three basic circuits as part of the design procedure. Thus R_1, R_2, in the OR gate, R_1, R_3, and R_5 in the bistable and R_1, R_2 and R_6 in the AND gate (see Figures 2-24, 2-27, 2-29 for circuit location of each resistor) are chosen in such a way that their correct value is achieved by trimming.

The final trimmed value of these resistors are not known. It is only necessary to know that in no case will any resistor be trimmed beyond 100% of its initial value. Therefore the initial values are chosen so that under no circumstance will it be necessary to trim a resistor by more than 100%. Trimming by 100% appears reasonable based on life test data for several trimmed resistors, as previously described.

Trimming is the last step in the construction of each circuit. A test set up has been devised which will facilitate the trimming. The test setup is very simple, requiring only one precision instrument, which is a digital voltmeter. The rest of the test setup consists of d-c power supplies, a pulse generator, a jig (see Figure 2-41) for holding the circuit being trimmed, and a box containing a multicontact switch with three current-monitoring resistors.

The switch affords the convenience of measuring any circuit voltage, as well as the voltage across the current-monitoring resistors.

The resistance of the current resistors has been accurately measured with a Wheatstone Bridge. Thus, by measuring the voltage across these resistors with the digital voltmeter, current values can be determined with a high degree of precision.

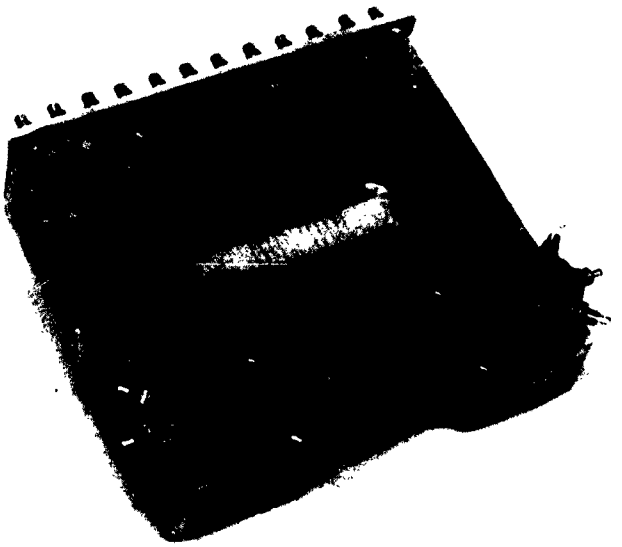


Figure 2-41. Trimming Test Jig (with wafer inserted) [8]

A trimming procedure has been developed for each of the three types of circuits involved in the 40-gate subsystem. The basic principals are discussed below.

As previously discussed, the object of trimming is to establish a relationship between the tunnel diode peak current and the quiescent bias point. Thus, immediately after trimming is complete, each tunnel diode bias (which is dependent on trimming) must be a known number of ma below the peak. These currents are designated as trim currents. They are measured by means of the current monitoring resistor discussed above.

The various trim currents are:

AND Circuit

(a) pulse buffer stage 2.45 ma.

(b) AND stage -2.9 ma.

(c) output stage 2.6 ma.

OR Circuit

(a) input stage 2.45 ma.

(b) output stage 5.3 ma.

Bistable Circuit

(a) set amplifier 2.45 ma.

(b) inverter driver 2.6 ma.

In addition to the two trim currents, the "bistable" circuit also has a requirement on V_T (see V_T in Figure 2-29). The value of V_T must be 55 mv when the current through TD_1 is 2.6 ma below the peak.

The trim currents are chosen in such a way that no combination of worst-case condition, including aging, will permit the quiescent bias point to come closer than 1.5 ma to the peak. On the other hand, the lowest quiescent bias level must permit a minimum of 7% overdrive, when the trigger current is the lowest available under any set of worst-case circumstances.

Expressions are given below which relate the trim currents to the worst-case conditions at the quiescent bias immediately after trimming is complete:

For either stage of the OR circuit the trim current

(I_t) is given by:

$$I_t = I_p (1-A) - \left[I_{TR}(1 + A) + I_{L_T} + I_b \right]$$

where: I_p is the specification tunnel diode peak current.

I_{TR} is the specification tunnel resistor mid point current.

A is the tolerance in hundreds.

I_{LT} is the sum of all leakage currents.

I_b is the current in the trim resistor immediately after trimming is completed.

I_b can be calculated from the fact that after aging the quiescent bias cannot be closer to the peak than 1.5 ma.

For the set amplifier in the bistable circuit the expression for I_t has the same form as for the or circuit.

For the inverter driver stage of the bistable circuit I_t is given by:

$$I_t = I_p (1-A) - \left[I_{TR} (1 + A) + I_b \right].$$

For the pulse buffer and output stages of the AND circuit, the form for I_t is identical to that given for the OR circuit. For the AND stage, however, I_t is given by:

$$I_t = I_{TR}\,(1 + A) + I_b + I_L - I_p\,(1-A)$$

4. Pulse Response of Plug-in Connector

This is a continuation of the work reported in IRR-14A, pp S107-S109.

A fast experimental vertical amplifier for the type 661 oscilloscope was used to enable the scope to respond to a step voltage in 100 picoseconds. Thus, it is now possible to see pulses close to 0.6 ns in duration with little distortion from the scope. As seen on the scope, the 10 to 90 percent risetime of the tunnel diode pulse generator used to observe connector response is 0.17 nanosecond.

Crosstalk in the plug-in wafer-coax connector was observed as a function of risetime (Figure 2-42). The data was taken with 25-, 54- and 75-ohm coax terminating both ends of the connector. As noted in the previous report, the back-cross pulse (toward generator) has the same polarity as the incident voltage while the forward cross pulse is opposite in polarity.

Reflection ratios for the connector terminated on both ends with 25-ohm coax versus incident voltage risetime are plotted in Figure 2-43. Observations of cross pulses using 50-, 54- and 75-ohm cable indicate that the transient reflected voltage will be zero for a cable of between 55 - and 60-ohm characteristic impedance.

Thus the apparent characteristic impedance of the connector is between 55 and 60 ohms. The curves of Figures 2-42 and 2-43 yield optimistic results for risetimes less than 0.5 ns since scope attenuation of a narrow pulse becomes significant in that region.

5. Mathematical Model of Plug-In Connector

A conventional "T" section was selected to represent the connector. The equivalent circuit is shown in Figure 2-44.

$$\frac{di}{dt}1 = \frac{2}{L}\left[2e_I - R_o\, i_1 - \frac{1}{C}\int (i_1 - i_2)\,dt\right]$$

$$\frac{di}{dt}2 = \frac{2}{L}\left[-R_o\, i_2 + \frac{1}{C}\int (i_1 - i_2)\,dt\right]$$

Since, $V_{in} = e_R + e_I$ it follows that,

$$e_R = e_I - R_o\, i_1$$

$$e_T = i_2\, R_o$$

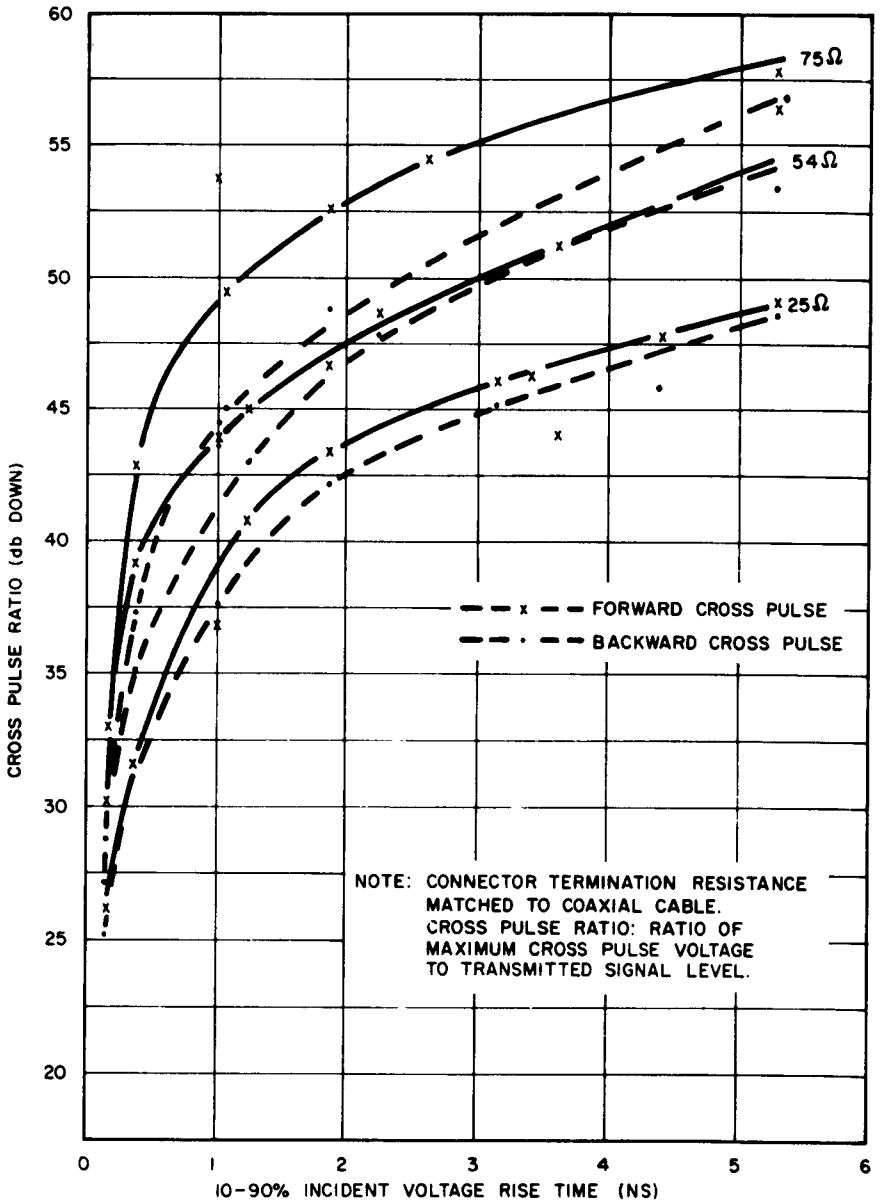


Figure 2-42. Cross Pulse Ratios of Plug-in Coax-Wafer Connector Versus Incident Voltage Risetime for 25-, 54- and 75-ohm Coax [8]

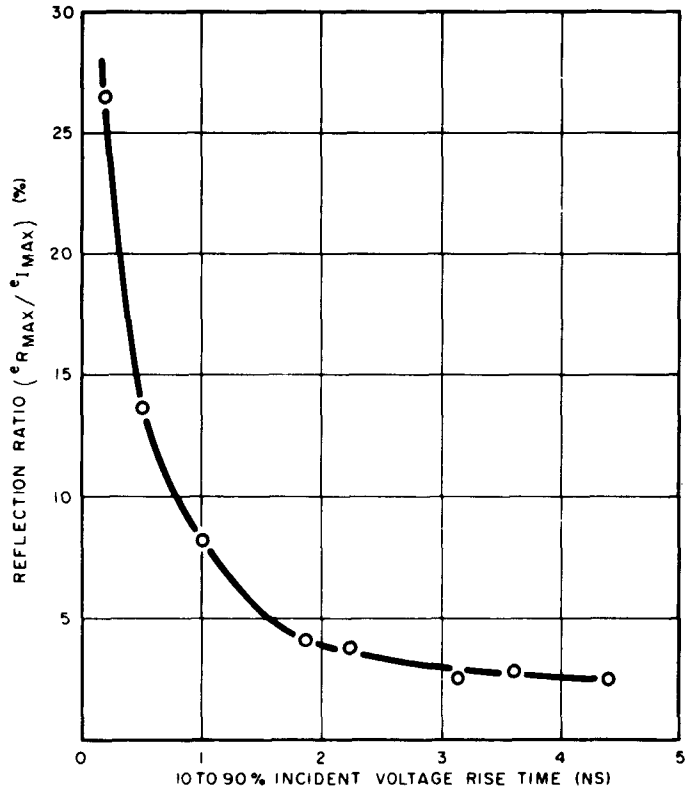
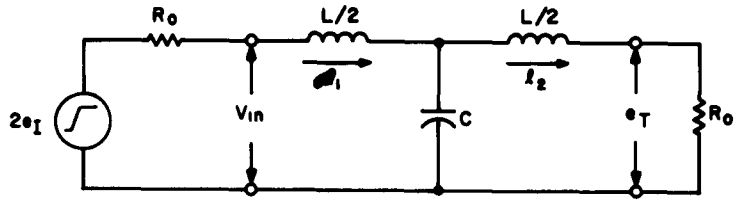


Figure 2-43. Reflection Ratio of Plug-in Connector as a Function of Incident Voltage Risetime with 25-ohm Cable Terminations [s]

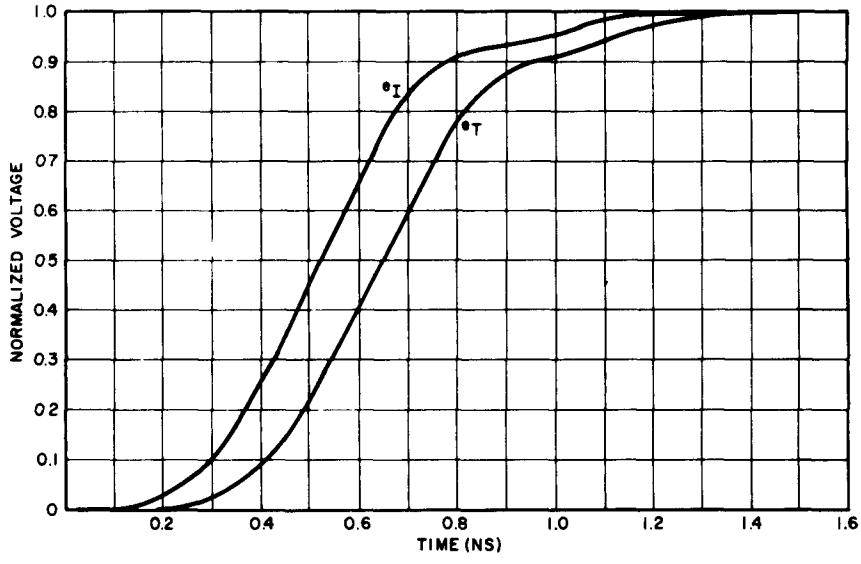
where e_I, e_T and e_R are the incident, transmitted and reflected voltages, respectively.

The equations were solved on the RCA 301 Computer taking advantage of sub-routines written for tunnel diode circuit computations.

The incident voltage waveform (Figure 2-44b) is the open connector reflected waveform as seen on the scope. Thus, the incident and reflected waveforms seen in Figure 2-44 are passed through the same lengths of cable and into the scope nullifying the effects of cable and scope distortion from the comparison. The experimental and computed reflected waveforms, based on a normalized incident voltage of one volt, are compared in Figure 2-44c.

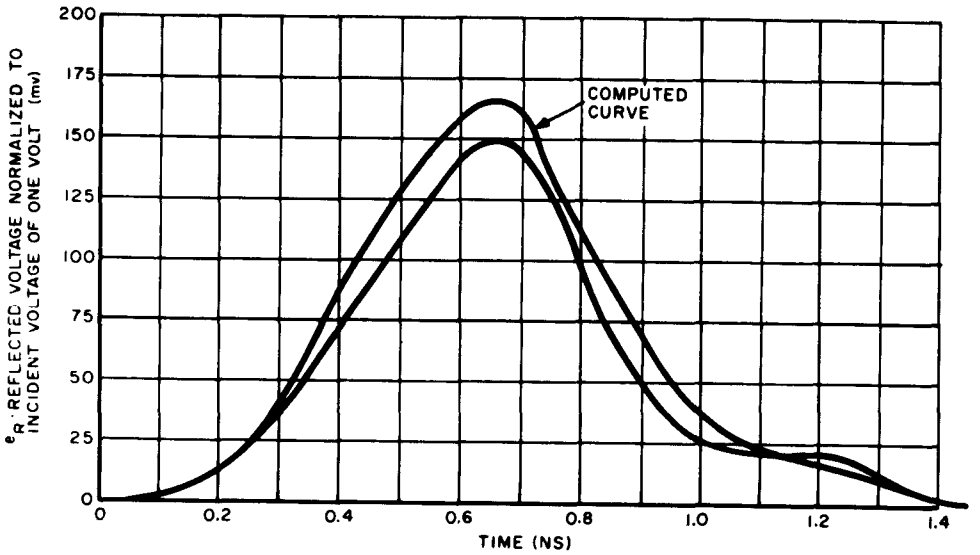


(a) Equivalent Circuit



(b) Incident and Transmitted Voltage Waveforms for $R_o = 25\,\Omega$; L = 5.5 nh; C = 1.8 pf

Figure 2-44. Plug-in Connector Circuit Model and Computed Waveforms [5]



(c) Comparison of Computed and Experimental Reflected Waveforms for R_o = 25 Ω; L = 5.5 nh; C = 1.8 pf

Figure 2-44. Plug-in Connector Circuit Model and Computed Waveforms (Continued) [s]

The connector delay was measured to be 0.11 ns and 0.13 ns for 54- and 25-ohm terminations, respectively. Under matched conditions, the characteristic, or image, impedance and delay of the "T" section are approximately,

$$R_I = \sqrt{\frac{L}{C}} \qquad T = \sqrt{LC}$$

Since 54 ohms is close to the matched impedance, the matched delay of the "T" section is about 0.11 ns.

The parameters of the connector used to compute the waveforms in Figure 2-44 indicate R_I equals 55 ohms and "T" equals 0.1 ns. The computed delay of 0.13 ns agrees exactly with the measured delay for R_o equal to 25 ohms. Thus, the measured and computed values of reflected pulse amplitude and width, connector delay, and characteristic impedance agree to within 10%. Considering the difficulty of using scope pictures to reproduce waveforms on the order of 30 mv or less in amplitude, the results are quite good. If two "T" sections were used instead of one, the results would most likely be more accurate.

6. Pulse Cross-talk in Micro-Strip Line

To gain insight into pulse crosstalk phenomena, a short study was made using micro-strip lines. The system tested is shown in Figure 2-45. The test set up is that used for the plug-in connector pulse response studies.

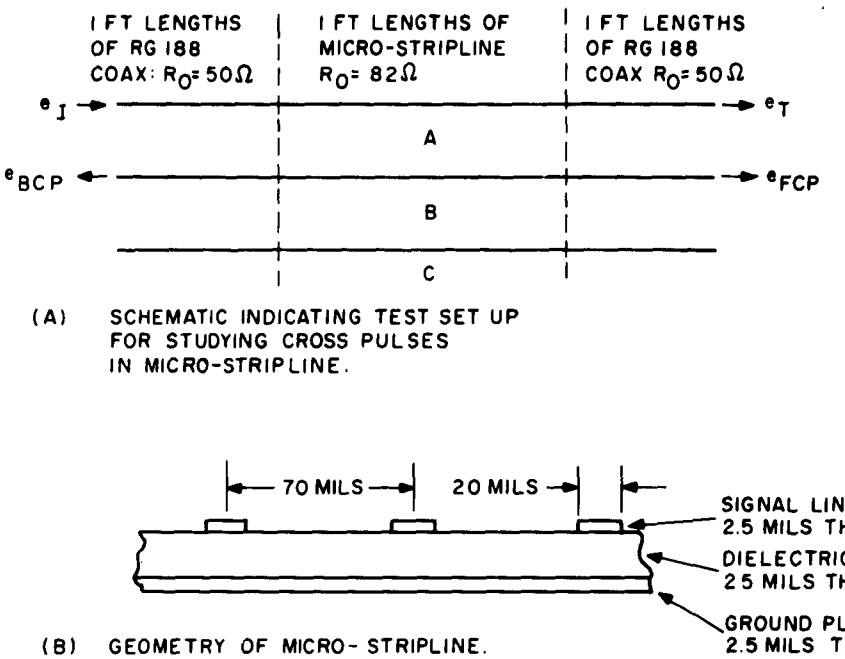


Figure 2-45. Details of Micro-Stripline [8]

Figure 2-46 indicates the response of the micro-strip line to a pulse much wider than the delay of the micro-strip line. The spike pulse seen at the end of the back cross pulse waveform is the reflected forward cross pulse, caused by the mismatch between the micro-strip line and the 50-ohm coax. The width of the back cross pulse is equal to twice the time delay of the micro-strip line. The increase in level of the forward cross pulse is caused by the reflection of the back cross pulse. e_{BcP} and e_{fcP} are respectively 29.7 and 15.5 db down from the transmitted voltage level. Cross pulse ratios one line removed (line "a" coupling line "c" in Figure 2-45) are 43.4 and 23 db in the backward and forward directions, respectively.

The response of the micro-strip line to a slower, narrow pulse is shown in Figure 2-47. The back cross pulse ratio is the same as that in Figure 2-46, namely 29.7 db. However, the forward cross pulse ratio is 21.7 db. Reflections from opposite ends of the line are compensated for in these ratios. Figures 2-46 and 2-47 together with other data indicate that the back cross pulse is an attenuated reproduction of the transmitted pulse. However, the forward cross pulse seems to be a function of the derivative of the transmitted pulse.

7. Logic Wafers

Typical wafers fabricated for use in the 40-gate subsystem are shown in Figure 2-30b. The construction detail of these wafers was described on pages S-111 and S-112 of IRR-14A. Approximately 31 wafers are in various stages of fabrication for the 40-gate subsystem with 6 of these tested and ready for use.

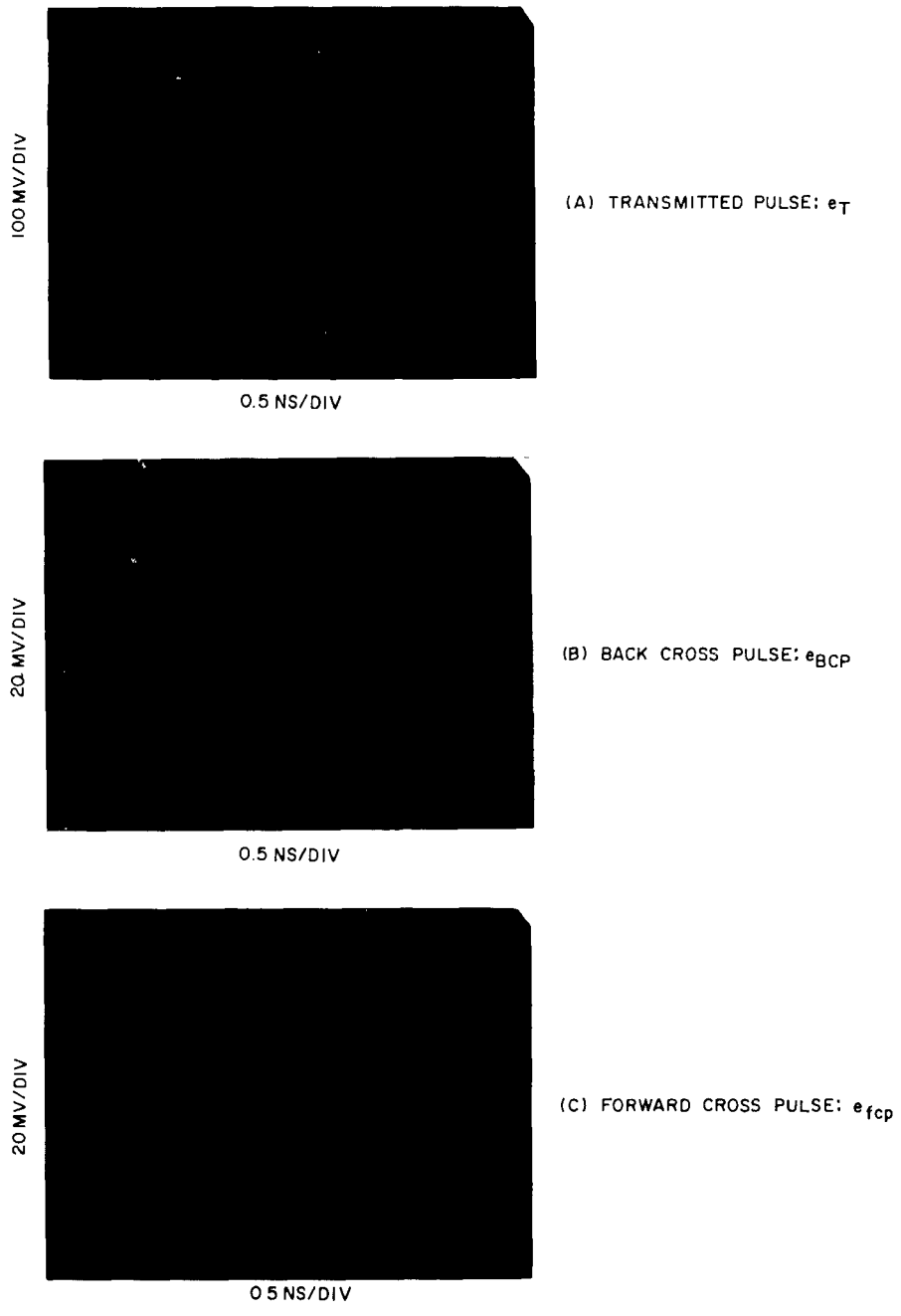
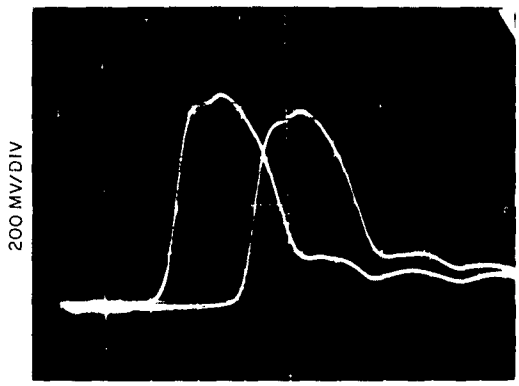
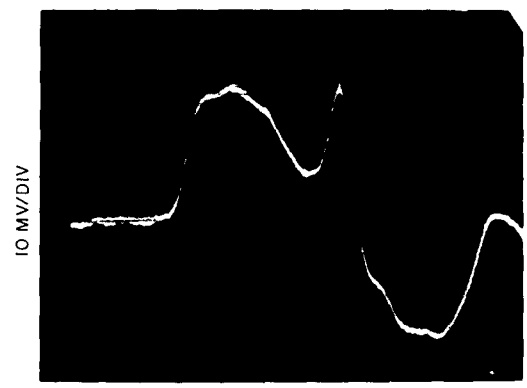


Figure 2-46. Response of Micro-Stripline to Wide Incident Pulse [s]



(A) LEADING. INCIDENT TO STRIPLINE
LAGGING: TRANSMITTED PULSE



(B) BACKCROSS PULSE

(C) FORWARD CROSS PULSE

Figure 2-47. Response of Micro-Stripline to Incident Pulse of Short Duration [s]

8. Frame Assembly

A prototype single-row frame assembly reflecting the packaging scheme to be used in the 40-gate subsystem is shown in Figure 2-48. This arrangement was discussed on pages S-112 and S-113 of IRR-14A. Figure 2-49 shows the wiring side (bottom) of the frame assembly.

A prototype frame connector and an improved model are both shown in Figure 2-50. In this design a number of terminals are disposed in the cross bar member of the frame assembly and positioned so as to allow their insertion into a horizontally positioned 12-pin wafer socket. The terminals are designed so that the ground and signal members are separated by a dielectric material. At one end of the terminal there is a suitable arrangement to permit soldering the shield and signal portion of a miniature coaxial cable. The other end of the terminal is arranged to permit proper insertion into a standard 12-pin wafer socket.

This terminal may also be redesigned for crimping or welding to the coaxial cable. The improved model shown in the photograph, containing only two terminals, has the added feature of being completely enclosed in a metal housing. In addition, each terminal is removable.

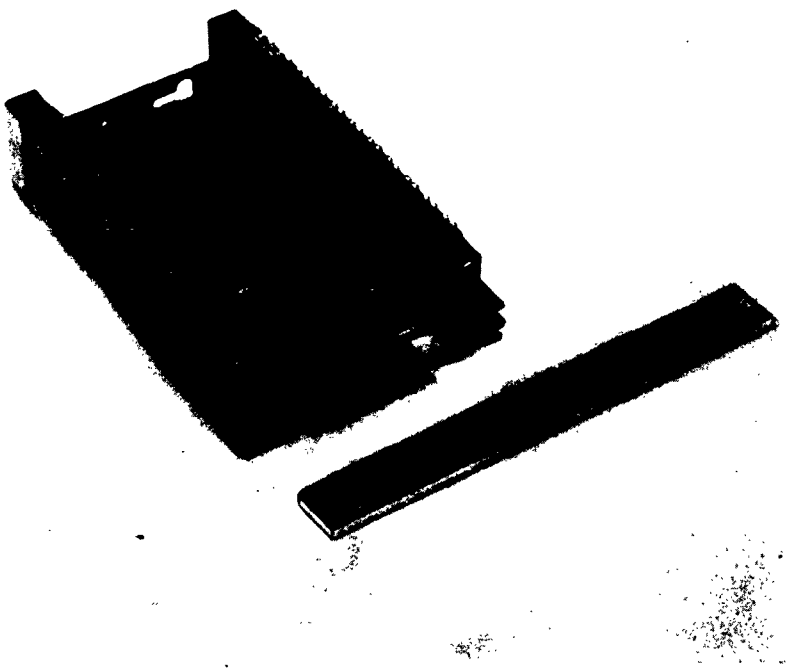


Figure 2-48. Frame Assembly [s]

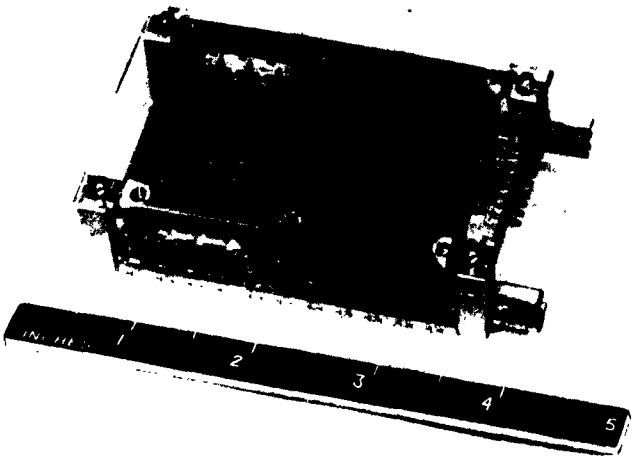


Figure 2-49. Frame Assembly, View of Wiring Side [s]

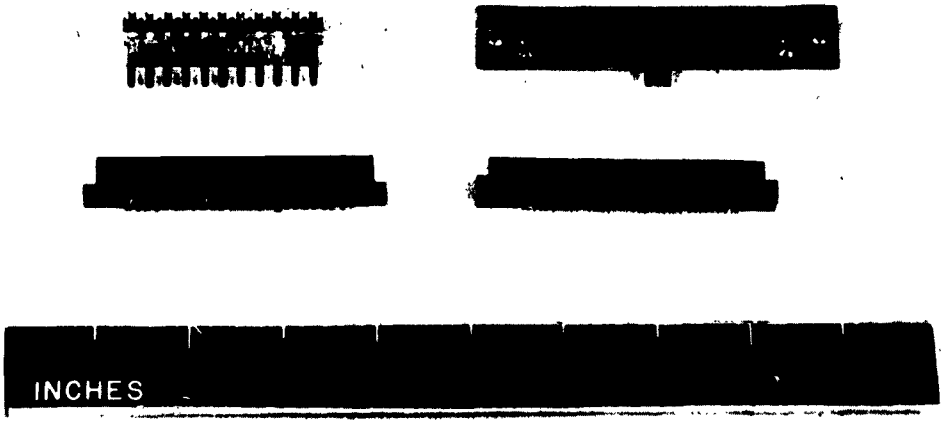


Figure 2-50. Prototype Frame Connector and Improved Version [s]

Figure 2-51 shows the details of interconnecting the main d-c distribution buss to the frame feeder buss system.

Shown in Figure 2-52 is a comparison of the 8-pin and 12-pin wafer connectors with their respective wafers inserted. The 12-pin connector is basically an improved model of the 8-pin wafer connector discussed in IRR-11A P. S62, with 12 contacts instead of 8 and considerably smaller.

The 40-gate subsystem frame assembly will be interconnected with miniature coaxial cable having a nominal impedance of 55 ohms and 31.5 ohms. The coaxial cable diameter will be 0.020 inch. Core material for 75- and 100-ohm impedance lines was obtained and sample quantities of coaxial cables are expected shortly for evaluation.

Two wafer test fixtures (one shown in Figure 2-53) were modified to accept the 40-gate subsystem wafers.

Several terminals for making a removable electrical connection between a semi-rigid coaxial connector and a connector or circuit board were investigated. A sectional view of a spherical coax terminal is shown in Figure 2-54. This terminal offers considerable flexibility of application, non-destructive removability of the coaxial cable assembly from the circuit, some impedance match to the cable, and freedom from rotation in its seat without shorting or loss of electrical contact.

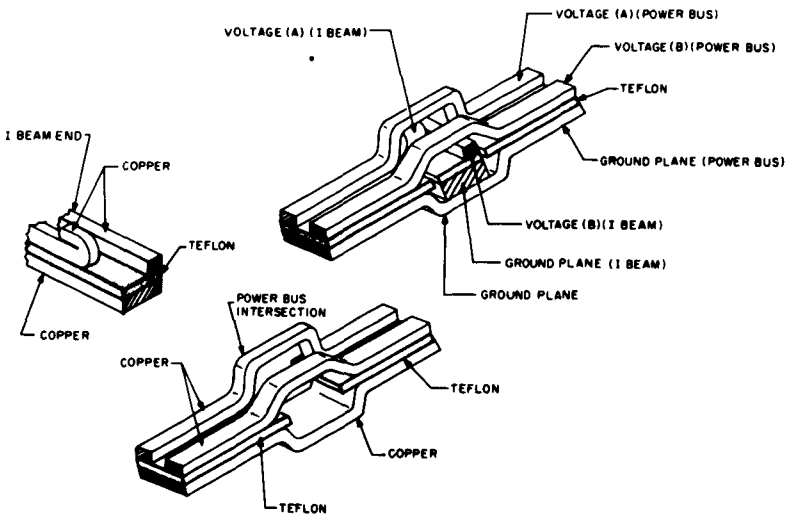


Figure 2-51. Horizontal Power Buss Connection [s]

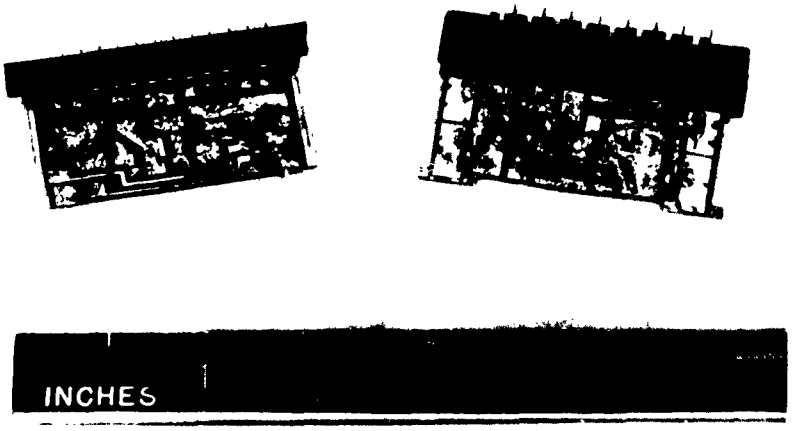


Figure 2-52. Eight-Pin and Twelve-Pin Wafer Connectors [5]

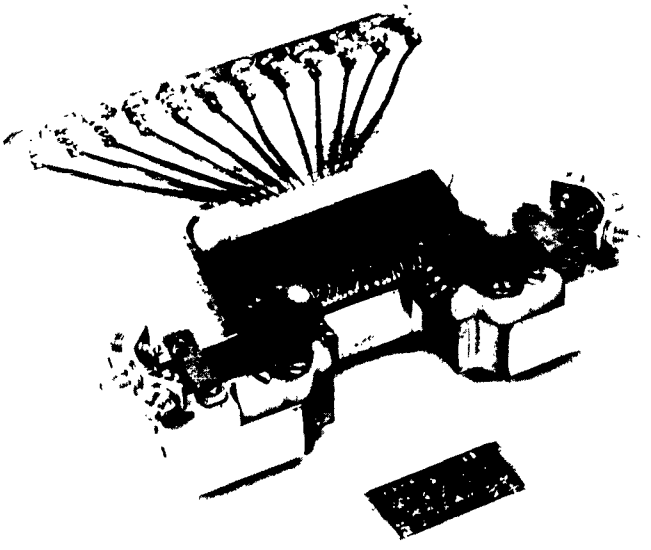


Figure 2-53. Wafer Test Fixture (wafer removed) [5]

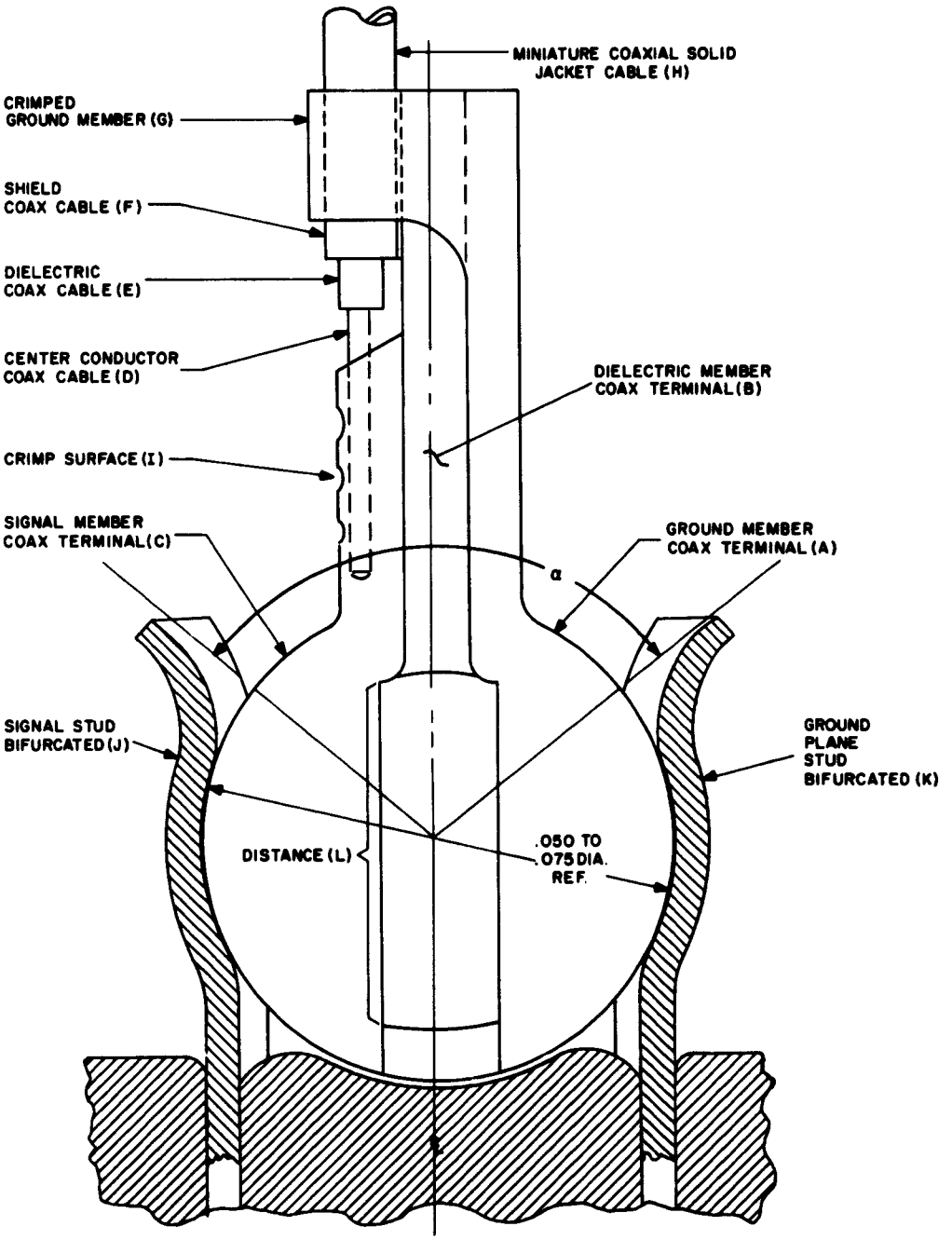


Figure 2-54. Details of Spherical Coax Terminal [8]

The spherical terminal is comprised of three elements: A, B and C. Elements A and C would be fabricated from a suitable contact material such as gold-plated hard copper. Element B would be fabricated from a suitable dielectric material. If the dielectric material selected is pliant and subject to cold flow, it may be reinforced by a border of ceramic or glass, also small disk or orbs of glass may be imbedded in the dielectric material. The three elements would then be bonded together with a suitable bonding agent. Although the figure shows a crimp-type connection between the coaxial cable and the terminal, a solderable or weldable connection may be made with a slight modification of the terminal.

In application, a spherical coaxial terminal is attached to both ends of a given length of interconnecting miniature semi-rigid coaxial cable. This cable assembly would then have its ends plugged into ball seats as shown in the figure. The ball seat may be attached to the edge of a circuit board or it may be fixed to the wiring side of a connector such as the 12-pin wafer socket.

It should be noted that a portion of the dielectric material extends beyond the spherical surface along distance L in Figure 2-54. The purpose of these ears is to limit the rotation of the terminal in its seat so as not to permit shorting of the signal element to the ground element.

Figure 2-55 shows a variation of a coaxial terminal. Although it does not have all the features of the spherical terminal, it does lend itself to thinner elements.

C. SUBSYSTEM IMPLEMENTATION

The 40-gate subsystem, shown in Figure 2-56, will be a 5-bit register capable of counting or shifting. The unit will be composed of 10 bistable wafers, 23 AND wafers, 4 OR wafers and 3 pulse load wafers. Wafer placement in the 4-column, 12-row frame is shown in Figure 2-57. Using the worst-case time delay figures for the logic circuits, it was determined that the maximum repetition rate for counting or shifting will be limited by the repetition rate of the circuits; therefore, a maximum rate of 300 mc for shift or count pulses will be possible. In the count mode of operation, the bistable output of the last stage will be available 9.4 ns after application of the count pulse.

Operation of this subsystem will check the circuits in a manner found to be the most critical in the 200 gate LIGHTNING Subsystem. That was the operation of the A register in a high-frequency shifting mode where some power supply disturbance was observed.

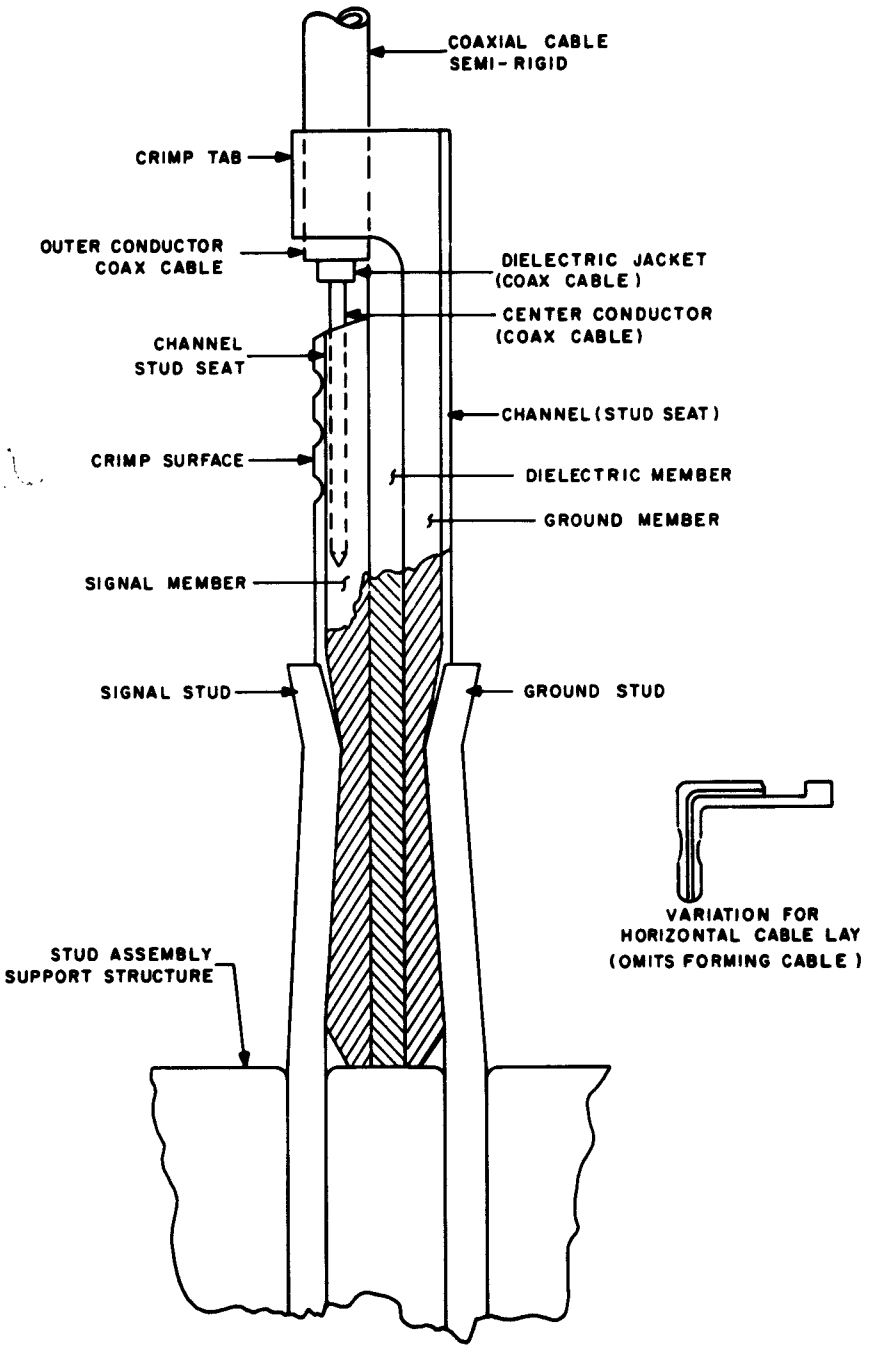
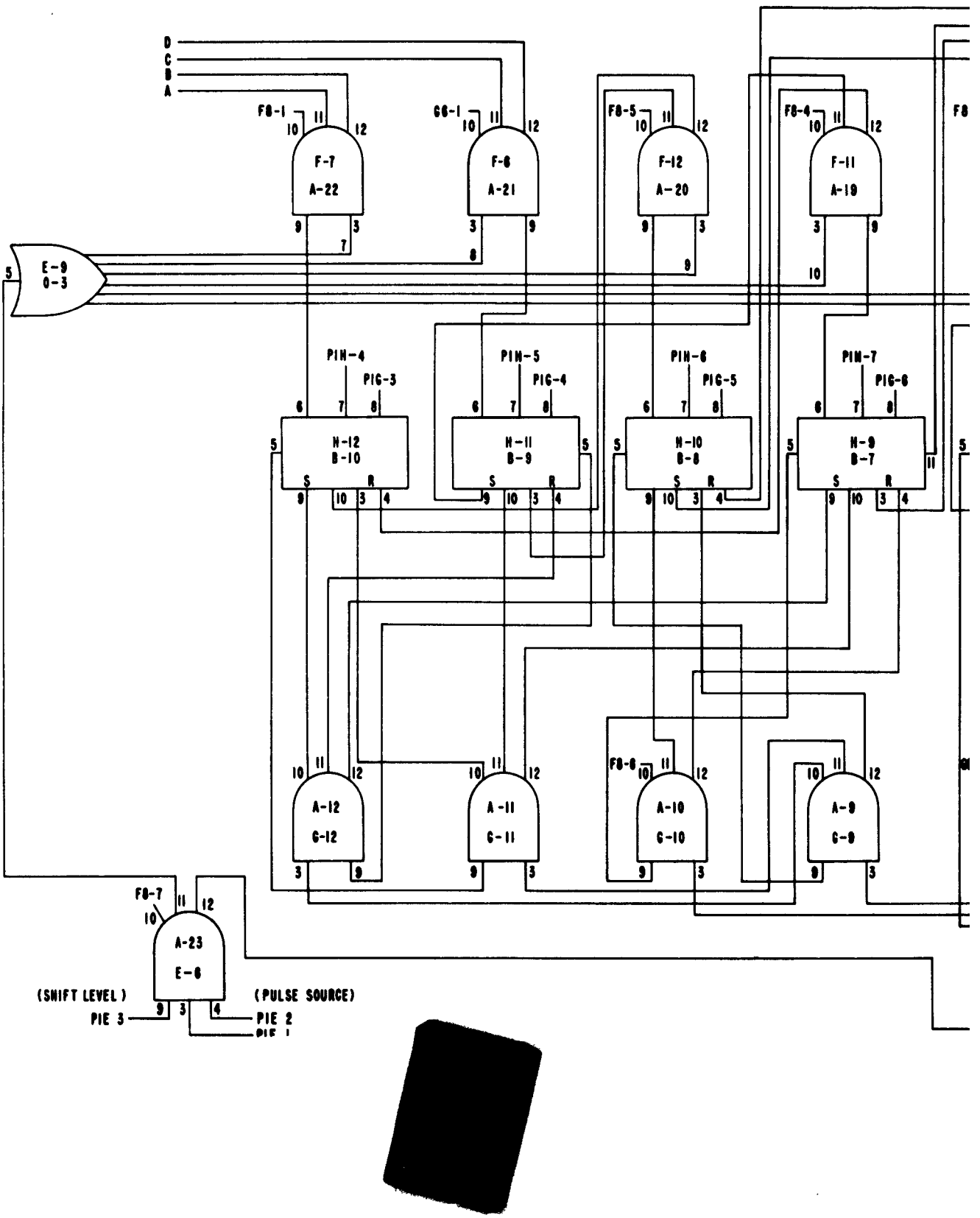
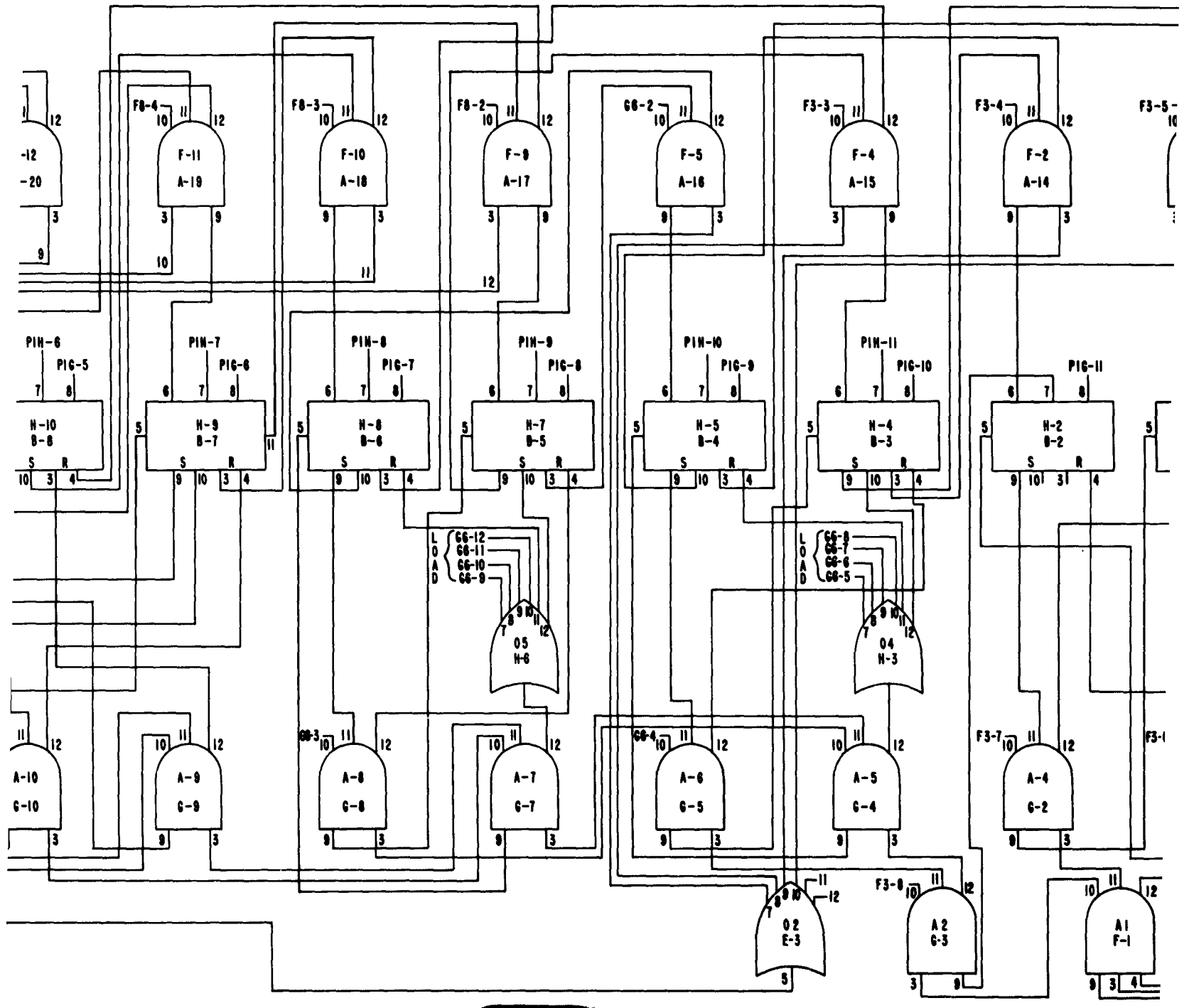


Figure 2-55. Variation of Coax Terminal (a)


D
C
B
A
F8-1
F-7
A-22
G6-1
F-6
A-21
F8-5
F-12
A-20
F8-4
F-11
A-19
E-9
0-3
PIN-4
PIG-3
H-12
B-10
PIN-5
PIG-4
H-11
B-9
PIN-6
PIG-5
H-10
B-8
PIN-7
PIG-6
H-9
B-7
S
R
A-12
G-12
A-11
G-11
F8-6
A-10
G-10
A-9
G-9
F8-7
A-23
E-6
(SHIFT LEVEL)
(PULSE SOURCE)
PIE 3
PIE 2
PIE 1



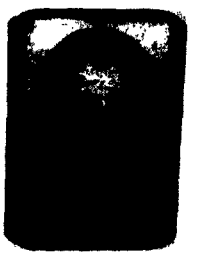


Figure 2-56. 4
Logic Dia

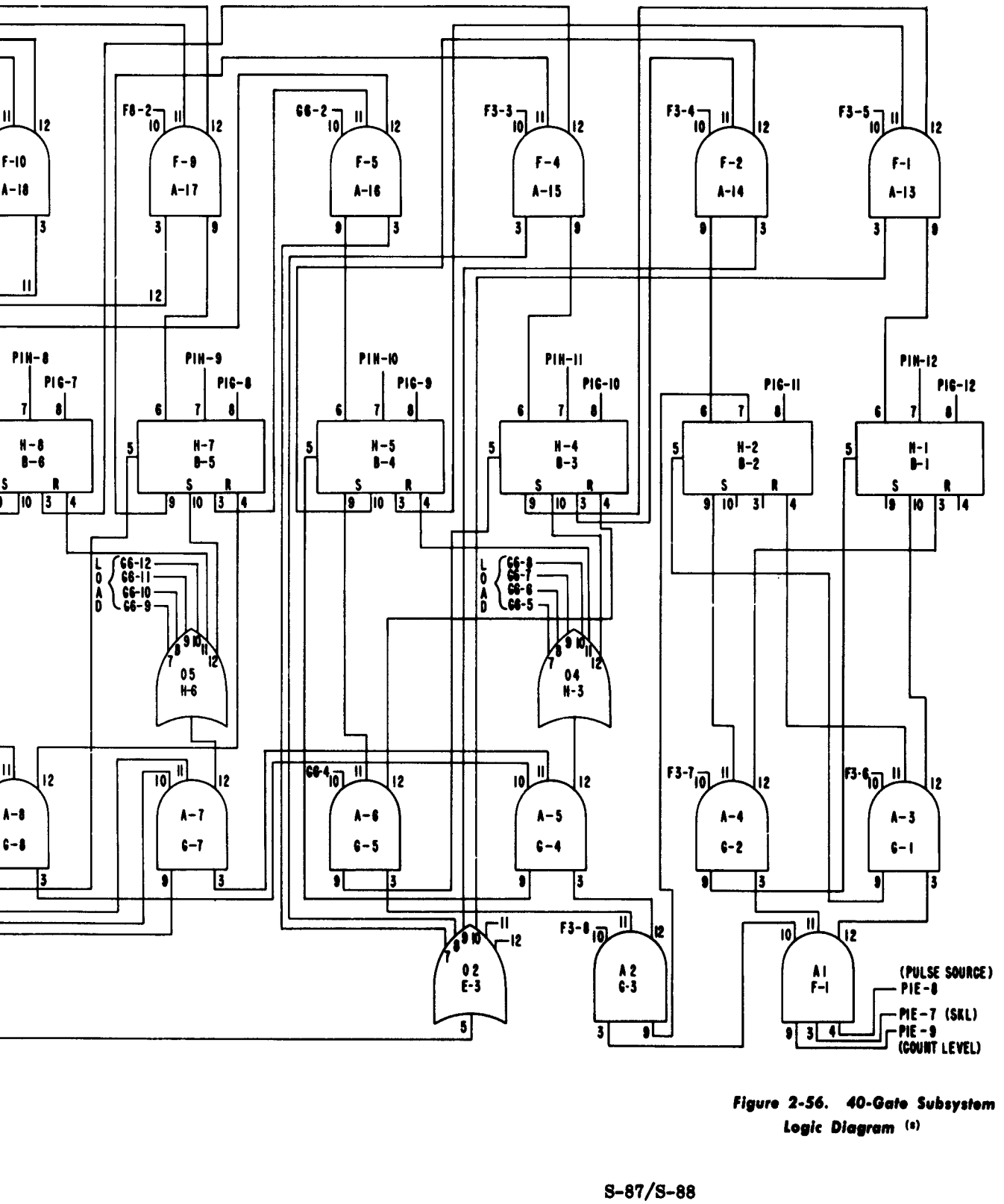


Figure 2-56. 40-Gate Subsystem Logic Diagram (a)

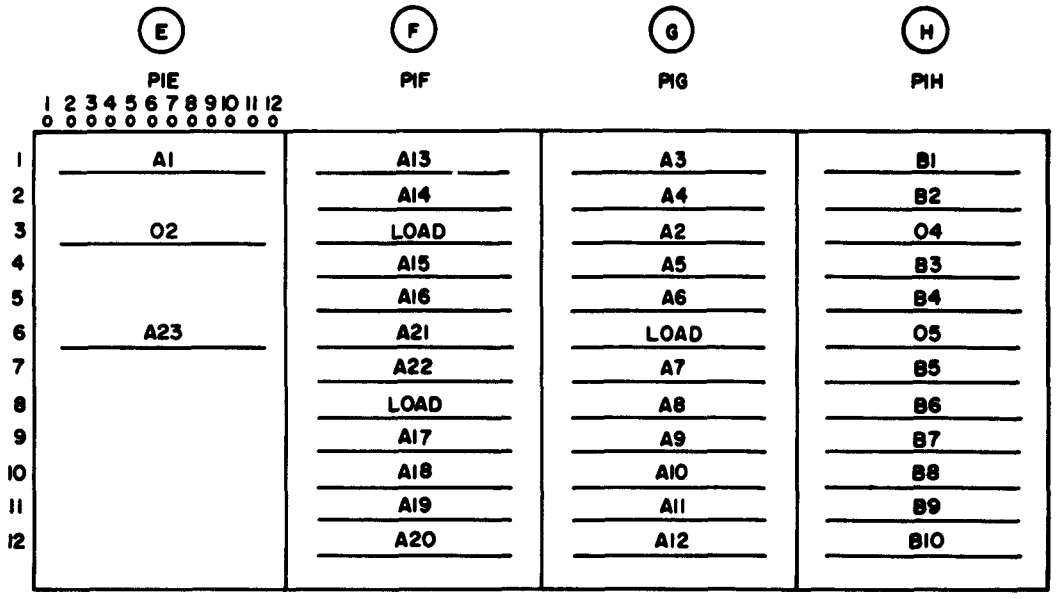


Figure 2-57. Wafer Placement in 40-Gate Subsystem [8]

Chapter 3. TECHNIQUE DEVELOPMENTS

SUMMARY

This chapter covers the work funded under Task IV of Phase III-B Extension, commonly referred to as "Circuit and Fabrication Completions Studies". Two alternative approaches to the triggerable flip-flop problem are discussed, the first is a more or less conventional method of interconnecting the basic logic gates presently designed for the 40-gate subsystem. The second is a considerably simplified approach which takes advantage of the rather specialized logic required for a triggerable flip-flop. This approach could result in a very much cheaper circuit.

The same general principle aforementioned applies to pulse stretching circuits as well; however, in addition to the two basic approaches a further split results in the categories of normal output pulse stretchers and inverted output pulse stretchers. These circuits are being investigated by simulation using a digital computer.

A new miniature cable connector has been developed which shows promise of being used as either a coaxial cable connector or a wafer connector. Actual crosstalk and reflected measurements were very favorable.

A sample of 50-ohm miniature flexible cable was received and tested. While the incremental inductance was somewhat higher than that of the solid-jacket cable, the losses were only slightly higher. This cable is quite flexible and is of sufficiently low loss to be useful where such flexibility is required.

Chapter 3. TECHNIQUE DEVELOPMENTS

I. PERSONNEL

The following personnel contributed to this phase of the project during the fifteenth quarter:

D. R. Crosby
M. E. Ecker
H. R. Kaupp
R. D. Yates
H. Ur

II. DISCUSSION

A. TRIGGERABLE FLIP-FLOPS

Tunnel diode triggerable flip-flops are customarily constructed out of two bistable circuits and some associated circuitry which includes at least two AND gates.

Figure 3-1 shows such an arrangement which consisted of the two bistable circuits. Each bistable circuit has a bistable stage, a set amplifier and an inverter circuit. The dotted lines show the mechanism necessary for making the flip-flop triggerable. This scheme is costly in number of circuits and sometimes the speed of operation.

Figure 3-2 shows an improved mechanism for achieving the same results. Under this scheme the set or reset input goes only to one of the set amplifiers of the bistable circuits. Assuming that one side was set from low to high state, its output is now used to trigger the inverter circuit of the second bistable and reset it to the low state. This cannot be done directly since the bistable level output could cause the inverter to produce an undesirable series of pulses. In order to avoid this situation, the bistable is coupled to the inverter through a capacitance. This allows only one firing of the inverter on the leading edge of the level produced by the bistable.

The coupling network to the inverter circuit causes complications because:

(1) The load presented to the bistable must be constant.

(2) Since the capacitor is connected to a diode at the input of the inverter, a discharge path must be provided to avoid the capacitor from charging to a voltage which is dependent upon the repetition rate.

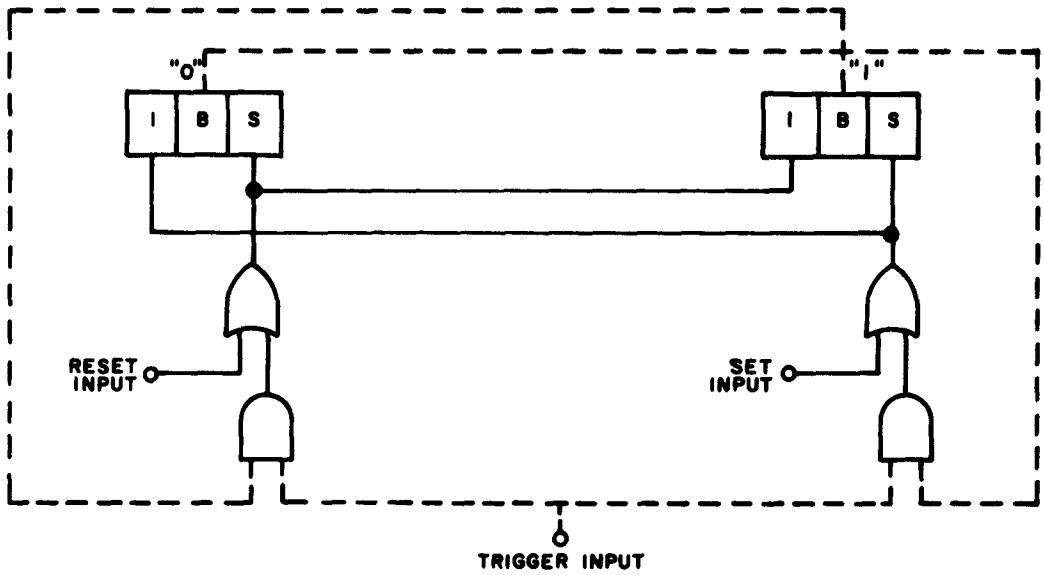


Figure 3-1. Conventional Flip-Flop With Provisions for Triggering (broken lines) [5]

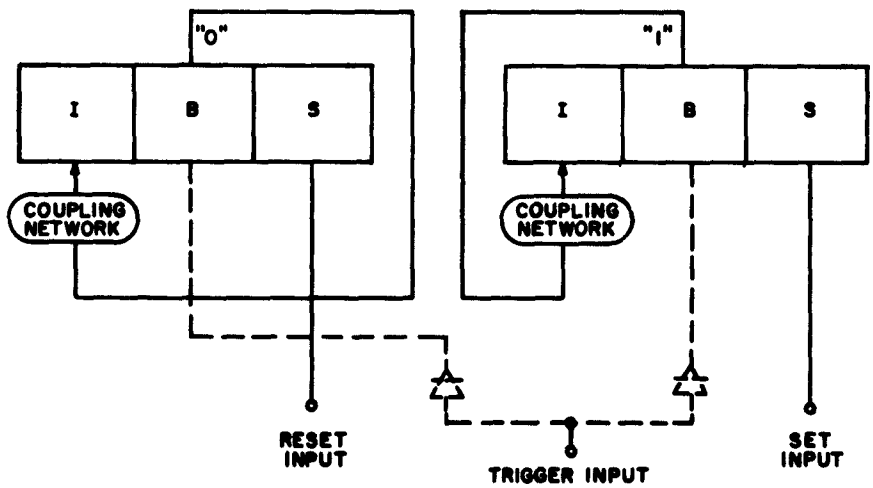
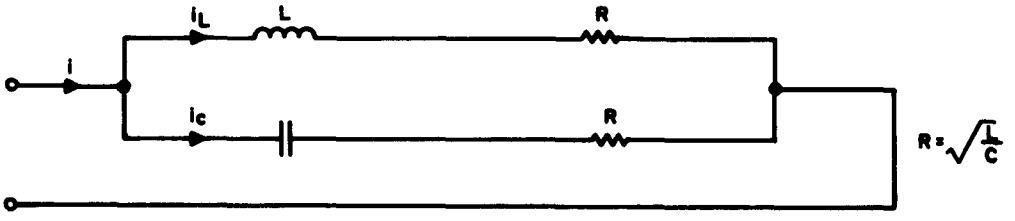


Figure 3-2. Proposed Triggerable Flip-Flop [5]

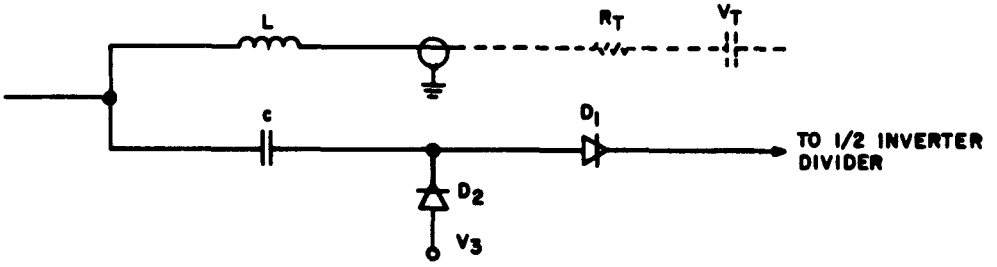
Figure 3-3 shows the coupling network. The principle can be understood by considering Figure 3-3a, the well-known constant resistance network. It presents resistance equal to R at all frequencies and for all transients. An interesting way to understand this action is by considering the response of this network to a step. Current i could be considered the sum of two currents, i_L and i_C, given by equations (1) and (2).

$$i_L = \frac{V}{R}\left(1 - e^{-\frac{R}{L}t}\right) \tag{1}$$

$$i_C = \frac{V}{R}\, e^{-\frac{t}{RC}} \tag{2}$$



(a) CONSTANT RESISTANCE NETWORK



(b) ADAPTED NETWORK

Figure 3-3. Coupling Network (a)

When examining the equations, it becomes obvious that when (3) holds, the total current is constant.

$$L/R = RC \text{ or } R = \sqrt{\frac{L}{C}} \qquad (3)$$

This is so because the decay of the current in the capacitive branch is exactly complemented by the build-up of the current in the inductive branch. The network of Figure 3-3b is the adaptation of that of Figure 3-3a to tie into the established circuitry. The inductive branch is simply a connection of an inductance tied through a transmission line into a termination circuit. The equivalent circuit is an inductance with a resistance connected to a constant voltage source. The capacitive branch is somewhat more complex: during the rise time it can be considered to be a series combination of a capacitance and a diode D_1 connected to V_2. For pulses of certain height, the network could be considered equivalent to that shown in Figure 3-3a if the impedance of the diode is substituted for its equivalent resistance.

During the fall time, the elements to be considered would be C and D_2. In the network 3a of Figure 3-3a, the two branches are connected in parallel, while in that of Figure 3-3b, they are tied to different d-c voltages. This should not affect the similarity since the difference would be a constant voltage present on the capacitance.

Thus, if one bistable is in the high state and the other one in the low state, triggering the set amplifier of the bistable in the low state reverses the situation. This would be true if the bistable diode would have been set by any mechanism. Thus, in order to achieve triggerable operation (namely, an arrangement by which the state of the flip-flop will alternate when a train of pulses is applied), a steering mechanism that will direct the set pulses to the bistable diode which is in the low state would be desirable. This is achieved by the network of Figure 3-4. The two tunnel diodes represent the bistable diodes of the two wafers, and they are connected to the same pulse through tunnel rectifiers as shown. Assuming that one of the tunnel diodes was in its low state, the pulses would set it to the high state. No current will flow to the high state diode. Had the state been reversed, current would have flowed to the other diode. Under the arrangement previously explained, setting the low-state diode to the high state causes the other bistable circuit to be reset to a low state.

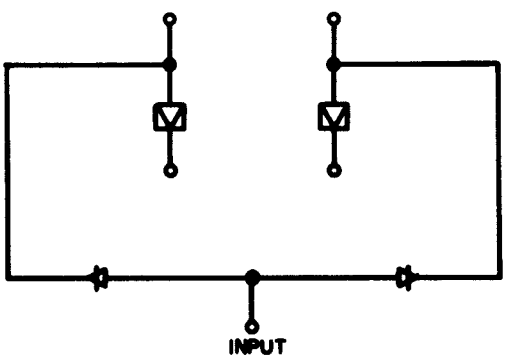


Figure 3-4. Steering Mechanism [8]

With normal pulse lengths and delays applied to the circuits, resetting would occur after the triggering pulse has elapsed and thus a race condition is avoided.

1. Counter Circuits

A triggerable flip-flop could serve as a counter circuit provided the carry output (pulse) is available every time the circuit changes in a certain direction, i.e., from "0" to "1" or from "1" to "0". The circuit would count up if the carry is produced when the circuit changes from "1" to "0" and count down (a less frequent requirement) if the carry is produced when the flip-flop changes from "0" to "1". This carry can be easily provided by utilization of a flip-flop output in the manner described before to trigger the trigger amplifier of a succeeding flip-flop stage.

Since the counter normally does not require both set and reset features, some components may be saved by constructing counters which recognize one of the set amplifiers on one of the bistable wafers as a trigger amplifier.

2. Laboratory Test

Since circuits of the 40-gate subsystem type were not available, this scheme was tried on wafers of the type used in the LIGHTNING Subsystem. The circuit consisted of two bistable wafers, and an OR wafer. The OR wafer was used as a trigger amplifier by virtue of connecting two of its outputs to the bistable diodes (no coupling diode on the bistable side). The coupling network into the inverter (Figure 3-5) was somewhat different than that of Figure 3-3b due to the difference in the types of circuit. Since a resistance was used in series with the capacitance, there was no need to provide a special path to discharge the capacitance on the trailing edge. (The scheme of Figure 3-3b is superior since it prevents false triggering of the inverter on negative pulses by direct coupling into the inverter, bypassing the inverter driver.) The laboratory experiment consisted of the following:

(a) A pair of pulses was applied to the trigger amplifier.

(b) One pulse was applied to the set side and one pulse (delayed) to the reset side.

Since the circuit is symmetrical, the set and reset terminals are interchangeable from a circuit point of view.

(c) One pulse was applied to the set amplifier and a delayed pulse was applied to the trigger input.

(d) Same as (c) but in reverse order.

The above procedure resulted in the waveform shown in Figure 3-6a. The dotted line in Figure 3-6b shows how the waveform would have looked had the input been repetitious. As indicated from Figure 3-7, a train of pulses equally spaced does not produce a square wave. This is because the transition from a high to a low state always lags behind the transition from a low to a high state.

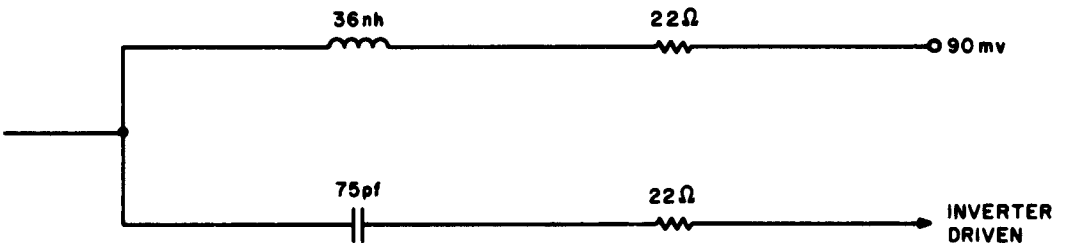


Figure 3-5. Coupling Network Used for Subsystem Circuit [5]

B. PULSE STRETCHING CIRCUITS

Due to timing problems, an AND gate can accept only one pulse; the rest of the inputs must be levels. In the case where a pulse has to be gated against a pulse, the practice has been to use the first one (timewise) to set a bistable circuit which produces a level against which the second pulse is gated. This procedure requires a considerable amount of circuitry, increasing both cost and delay. It may also require timing pulses or a delay mechanism in the reset circuitry.

In order to avoid this complication, pulse stretchers are proposed. Pulse stretchers could produce a long duration pulse to be used in lieu of the AND gate level input. The pulse stretcher output would have to be compatible with the level transmission lines and loads

Two kinds of pulse stretchers are contemplated.

(1) output normally low - with an input pulse, becomes high for a duration of several nanoseconds.

(2) the output normally high - with one input pulse, becomes low for a duration of several nanoseconds.

The duration would depend on the requirements of the logic design and conceivably several durations could be obtained by selecting proper inductances. Since components of the "40-gate" type were not available, the investigation has centered on paper design followed by computer simulation. It has been aimed to use, as much as possible, components, circuitry and wafers to be utilized by the 40-gate subsystem.

A first try for the pulse stretcher of type (1) above was to increase the inductance of the last stage of a standard six output OR gate while using a load line similar to that of a bistable circuit. The schematic of the simulation is shown in Figure 3-7. The results are shown in Figures 3-8 and 3-9. These results are not very encouraging, due

(a)

1 NS/DIV

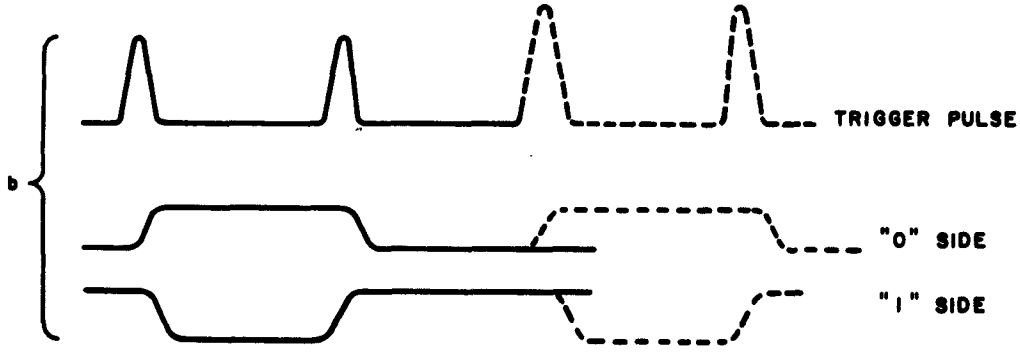


Figure 3-6. Flip-Flop Output Waveforms [a]

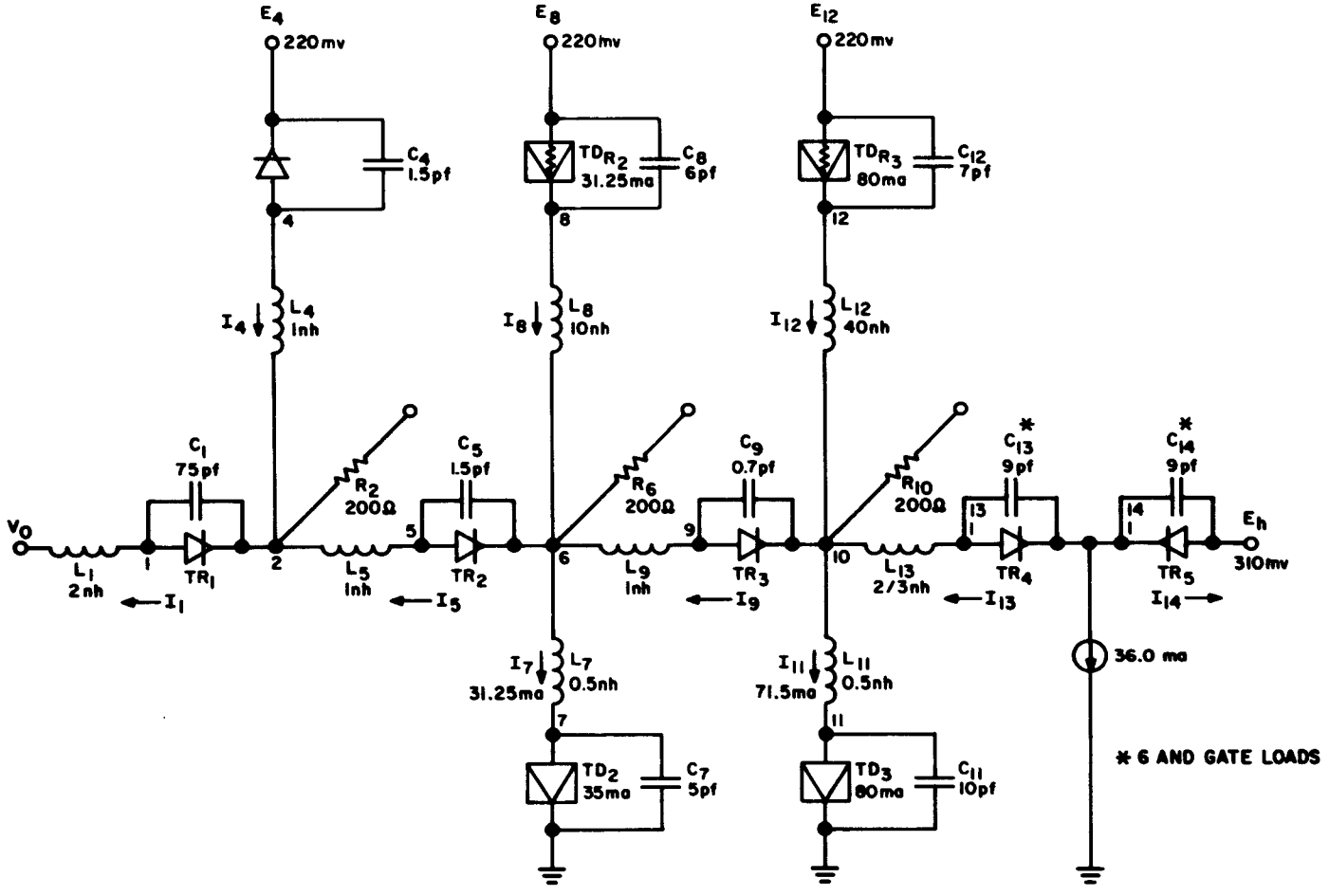


Figure 3-7. Circuit Used for Simulation [8]

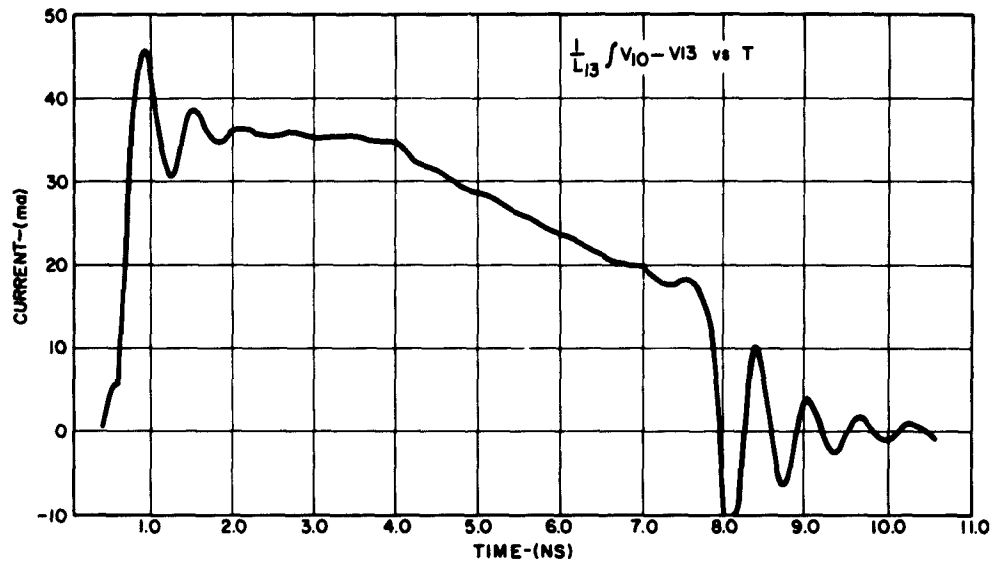


Figure 3-8. Output Current Waveforms [s]

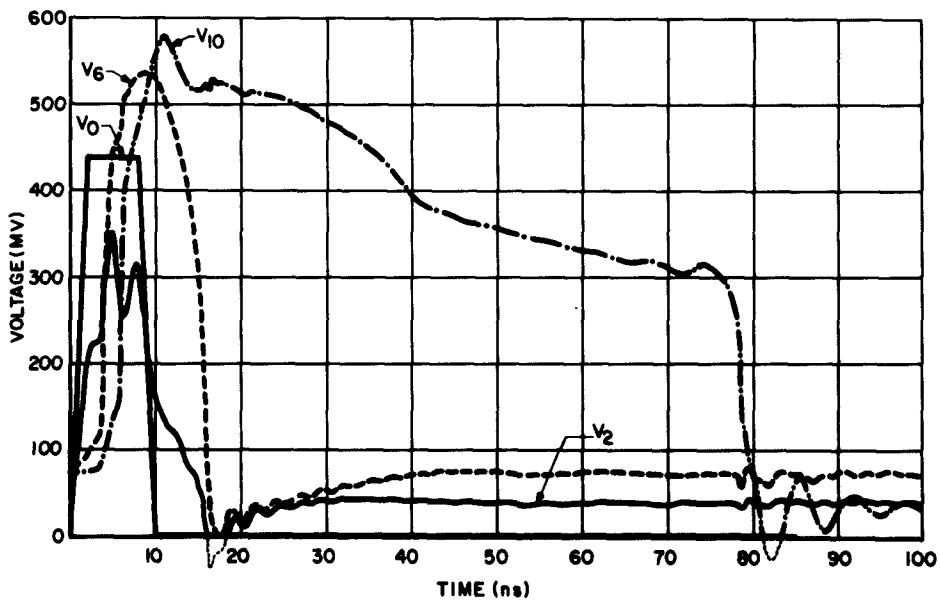


Figure 3-9. Voltage Waveforms [s]

to the fact that the useful time is only a fraction of the total time between two possible input pulses. This can be seen best from the waveform showing the current at the output. The "lost" time is composed of two portions:

(1) The time after the voltage at the output is decayed below the minimum useful output and the reset time, and,

(2) The recovery time.

While it is desirable to reduce both as far as possible, (1) is the least desirable. This is so because during that time no AND operation is permissible since gating against that voltage would be ambiguous. (2) above does not possess this ambiguity. The only objection is that time may be spent if it is desirable to pulse during its duration.

Utilization of a different variation of a monostable circuit will be tried to improve the difficulties mentioned above. It is recognized, however, that certain recovery time would be always present.

1. Inverting Pulse Stretcher

This pulse stretcher is of the type denoted previously by (2). The circuit being investigated is an adaptation of the bistable circuit. It is done by making the bistable diode monostable at the high state, utilizing the inverter as a trigger. This circuit is also being investigated by simulation on the digital computer.

C. MINIATURE COAXIAL CABLE CONNECTOR

A new miniature coaxial cable connector has been developed. The basic connector is shown in Figure 3-10. Placement of the coaxial cable and the mating of two connectors is illustrated in Figure 3-11.

Although the basic purpose of this device is to interconnect miniature coaxial cables, it is also applicable as a wafer or edgeboard connector. Furthermore, the connectors may be aligned in a frame, or cradle, to mate a large number of cables simultaneously.

Electrically, the cable has many advantages. Because of its lapping feature the connection can be made extremely short, thereby limiting reflections. Then, too, the apparent characteristic impedance of the connector can be varied by changing the thickness or type of dielectric material used.

If desired, the connector can be completely enclosed by being constructed with sides. When using the connectors in groups, the aligning frame can supply shielding to reduce crosstalk between adjacent connections.

Preliminary test results are favorable. With two connectors held together as they would be in a frame to frame connector, cross pulses were 44 db below the transmitted signal level. The peak of the transient pulse reflected from the connector was 35 db below the signal level. For comparative purposes, the crosstalk between adjacent connectors of the plugable wafer-coax connector used in the present LIGHTNING

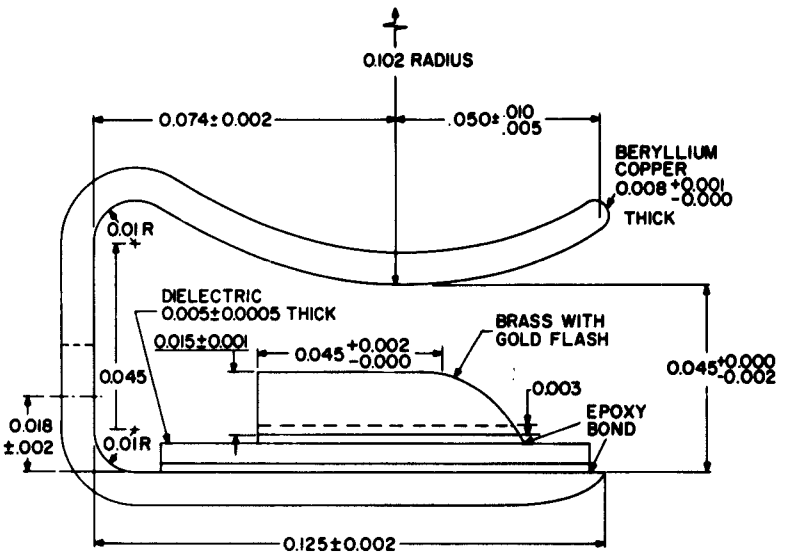


Figure 3-10a. Details of Coaxial Cable Connector [a]

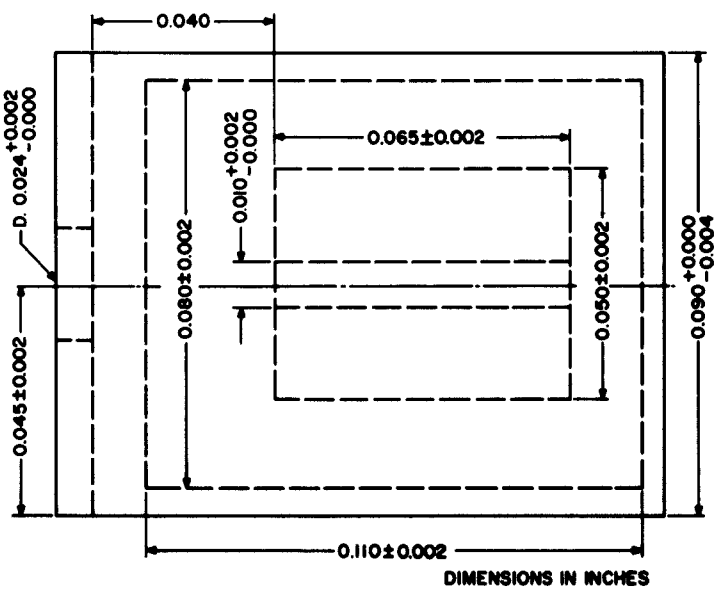


Figure 3-10b. Details of Coaxial Cable Connector [a]

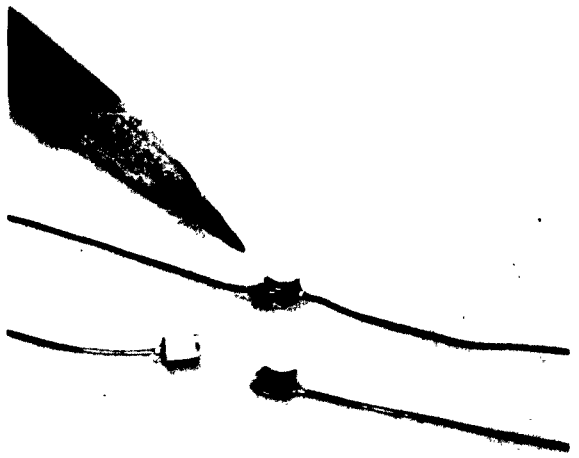


Figure 3-10c. Details of Coaxial Cable Connector [s]

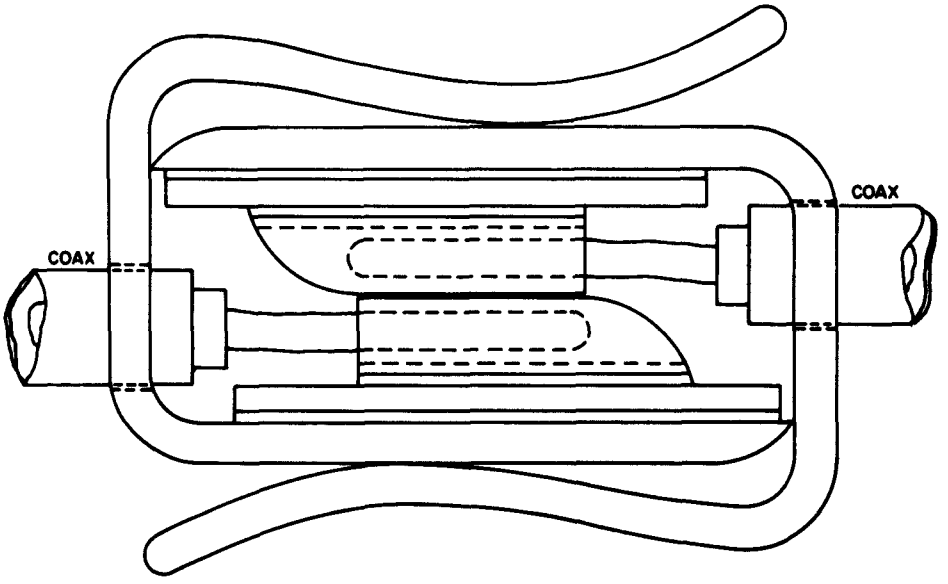


Figure 3-11. Details of Coaxial Cable Connector, Shown Mated [s]

Subsystem are 31 db down while the reflection is 15 db down. The response of both connectors were observed on a Tektronix type 661 scope (0.35 ns rise time). The rise time of the incident signal as seen on the scope was 0.4 ns. The cable used was the miniature solid-jacket 25.7-ohm coaxial cable (outside diameter of 20 mils) which is used in the LIGHTNING Subsystem.

D. FLEXIBLE MINIATURE COAXIAL CABLE

A sample of 50-ohm miniature cable was received and tested. The cable has a severed outer conductor, making it flexible. The core material is that used in the drawn copper jacket coax; diameters of the inner conductor and teflon dielectric are 5 and 16 mils, respectively. The outer conductor (a strip of silver-plated copper approximately 30-mils wide and 3-mils thick) is wound helix fashion over the teflon core. The outer conductor is then encased in a Milene jacket.

The characteristic impedance of the cable was measured by two different techniques and found to be 63.5 ohms (within two percent). Cable attenuation, measured by the "essential insertion loss" method, is: 1.17 db/ft at 0.8 kmc, 1.26 db/ft at 1 kmc and 1.79 db/ft at 2 kmc. The losses of a 50-ohm cable with a 5-mil inner conductor and solid-copper outer jacket would be 0.84 db/ft at 1 kmc.

Upon inspecting the sample piece of cable, it was found that a continuous gap of more than 2 mils existed between adjacent helical segments of the outer conductor. Thus, the current traveling on the outer conductor was forced to follow a helical path, increasing the inductance per unit length.

The effective propagation velocity of the cable was determined by observing the delay of a pulse through a length of cable. It was 6.06 inches/ns. However, the propagation velocity in the dielectric teflon is 8.15 inches/ns. Assuming that the change in propagation velocity ($V = 1/\sqrt{LC}$) is due only to the change in inductance, the square root of the inductance will increase by the ratio 8.15/6.06 = 1.34. Hence, the characteristic impedance of the cable will increase by a factor of 1.34, making it 67 ohms instead of the intended 50 ohms. This proves out the 63.5-ohm reading previously made.

Electrical discontinuities, seen as reflections, are introduced by squeezing and handling the cable - especially near a common ground plane. The cable is quite flexible and most likely will be acceptable if the outer conductor is overlapped. However, there may be some other applications for the cable in using the non-overlapping helical outer jacket to obtain higher characteristic impedance in a small cross-sectional area.

Chapter 4. INTEGRATED TUNNEL DIODE MEMORY SUBSYSTEM

SUMMARY

This program has resulted in a significant advance in the technology of microminiature tunnel devices and film resistors to very close tolerances. It has also shown that such devices could successfully be integrated into one small package (.030 inch x .030 inch x .060 inch). However, the small yield of each device, imposed by the close tolerances to which the individual units must be made, results in an integrated device which is economically unfeasible. Nevertheless, the small individual devices developed during this program were connected to show the feasibility of forming a circuit (memory cell) which is comparable in size to that originally specified as an objective (.060 inch x .060 inch x .060 inch).

Chapter 4. INTEGRATED TUNNEL DIODE MEMORY SUBSYSTEM

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II. DISCUSSION

The development of micro-miniature GaAs tunnel rectifiers, Ge tunnel diodes, and evaporated film resistors, for incorporation into an ultra-small (by present tunnel device standards) memory circuits, was successfully completed during this quarter. This completed the work on this task of the program. Therefore, in addition to describing the results obtained during this quarter, the work performed earlier in the program is also summarized.

The tunnel diode memory subsystem has been described in previous progress reports. A single word contains 32 bits or cells, each cell consisting of a GaAs tunnel rectifier, a germanium tunnel diode, and a resistor, connected as shown in Figure 4-1. The basic objective in the development of the integrated memory subsystem has been to evaluate the economic feasibility of producing either a single integrated memory cell (i.e., tunnel diode, tunnel rectifier and resistor), or a group of integrated cells, in a single package. During the first quarter, it was established that a group of integrated memory cells was economically unfeasible, and work during the second and third quarters was directed towards the development of a single cell. The mechanical details of this cell are shown in Figure 4-2. The tunnel diode and tunnel rectifier were inserted in a ceramic package whose outside dimensions were .030 inch x .030 inch x .060 inch. A film resistor was deposited on the outside of the package. Where required, interconnections were made using metallization. This is described more fully below.

During the first quarter, work centered about three major problems. The first, how to etch each individual tunnel diode or tunnel rectifier without affecting the electrical characteristics of neighboring units, was solved satisfactorily. It was found that a tunnel diode could be completely protected from the etchant by covering it with a suitable wax. Apiezon wax dissolved in trichlorethelyne (TCE) was applied to the diode. The TCE evaporated rapidly, leaving the diode completely covered by the wax,

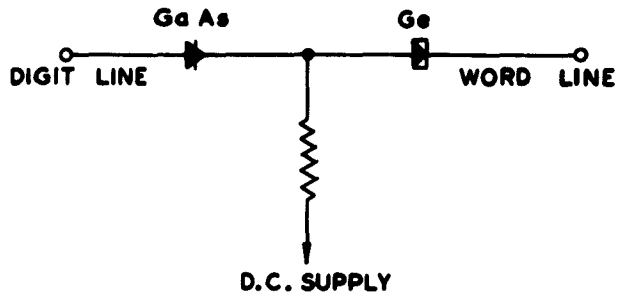


Figure 4-1. Basic Mercury Cell Circuit [a]

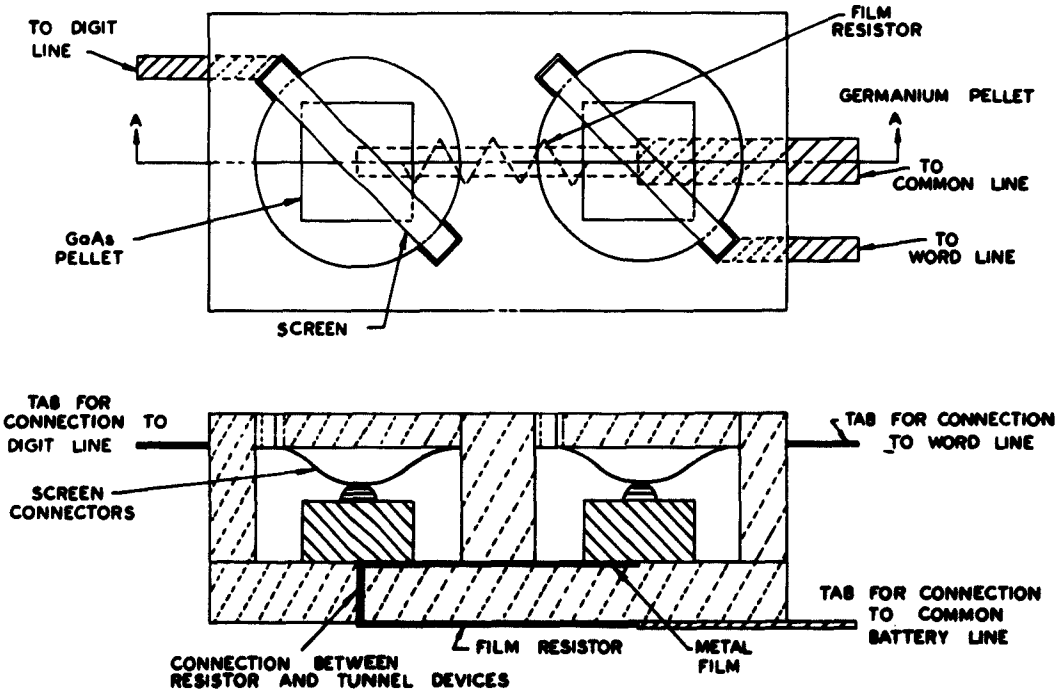


Figure 4-2. Details of Memory Cell [a]

which is impervious to the etch solution. The second problem, also satisfactorily solved, was the development of a package suitable for integrated devices in a strip transmission line circuit. The package developed is that shown in Figure 4-3a.

The package was made of high-alumina ceramic using molybdenum-manganese metallizing for conducting paths and semiconductor mounting areas. The ceramic is built up from alumina-loaded sheets of thermoplastic vinyl which are laminated together under heat and pressure and sintered to a dense ceramic. Wherever metallic areas are desired, such patterns are "silk-screened" on the sheets using a molybdenum-manganese paint. If such areas are to be within the body of the ceramic, then other sheets are laminated over the ones bearing the metal pattern. Holes are punched in the unsintered sheets using ordinary metal-working dies. Sheets having holes are laminated to sheets without holes to form cavities with bottoms. Details of this laminating process are shown in Figure 4-3b. Two such cavities, with appropriate metallizing, were used as a "unit cell" of the integrated memory subsystem. The use of individual cavities facilitates individual etching of the diode and rectifier.

The third problem involved the development of a tunnel diode, a tunnel rectifier, and an evaporated film resistor, all meeting the required electrical specifications and suitable for the package and individual etch techniques which were developed.

Some experiments were carried out to form a germanium-gallium arsenide heterojunction. Such a junction would have permitted the fabrication of both the germanium tunnel diode and the gallium-arsenide tunnel rectifier directly on one germanium wafer. The results of these experiments, however, indicated that it would be extremely difficult to make devices to the desired specifications using the heterojunction technique. It was therefore decided to make germanium tunnel diodes and gallium-arsenide tunnel rectifiers individually. Furthermore, the results of the etching experiments described above showed that two diodes in close proximity could be etched without interaction.

The dimensions of the pellets required for the integrated package is about .010 inch square, instead of the .020 inch or .035 inch size with the two conventional packages. Moreover, the small size of the overall structure, and the necessity of processing the individual devices without affecting one another, led to yield problems which made it extremely difficult to fabricate a finished cell in which all three elements were within the required specifications. Nevertheless, during the second quarter, several units were made which came quite close to meeting these specifications.

Figure 4-3a shows a typical memory cell made during this period. Of the three elements, the film resistor proved to be the most satisfactory. The resistors were made during this period by the evaporation of 80-20 nickel chromium alloy. Deposition was controlled to produce a sheet resistance of 300 ohms per square, which corresponds to a film thickness having zero temperature coefficient on large area alumina substrates. An evaporated silicon monoxide layer was then deposited over the resistor to protect it from oxidation. The units were aged at a temperature of

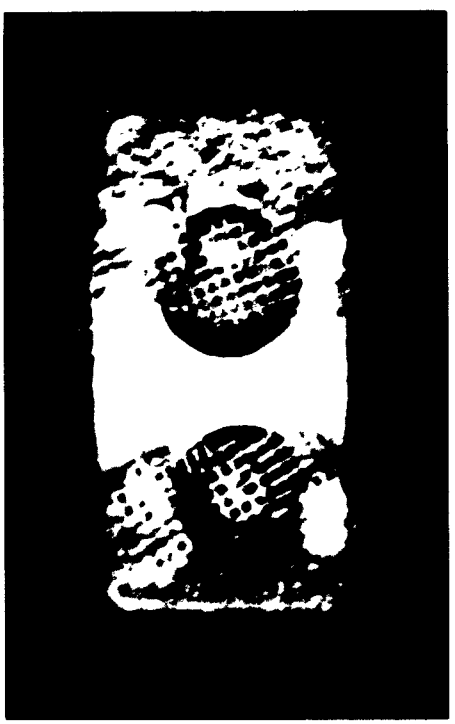


Figure 4-3a. Memory Cell Packaging [5]

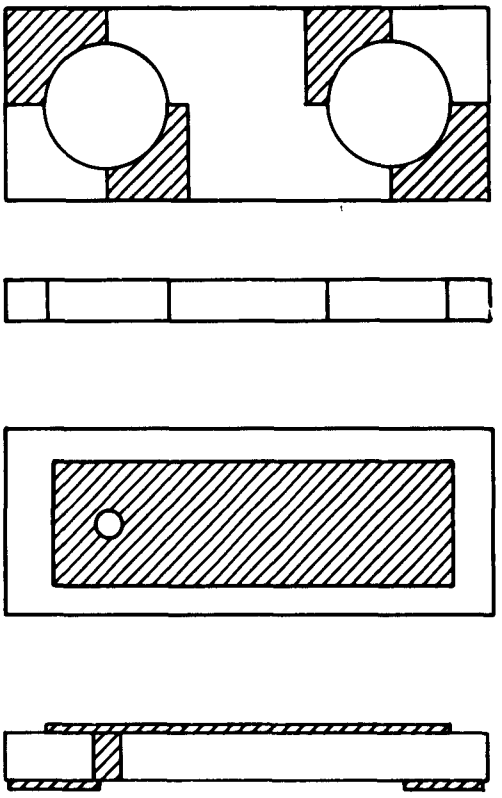


Figure 4-3b. Laminations for Package of Figure 4-3a (crosshatched areas are metallized regions) [8]

150°C for three days, and then adjusted to a value of 2,000 ohms ±1% by means of a precision air abrader. This process removed some of the silicon monoxide protective coating, so another layer of silicon monoxide was then evaporated over the resistor.

By the end of the second quarter, it was demonstrated that single cells were feasible. However, it appeared doubtful that such cells could be made economically.

During the third quarter, the work was directed towards improving the yield of satisfactory cells. However, it became apparent that the present state-of-the-art for tunnel diode technology did not permit the economic fabrication of such memory cells, and some attention was given to alternate means for achieving a low-cost, small-size, high-speed tunnel diode memory subsystem.

It was obvious that the low yield of the integrated cell could be avoided by connecting individual components directly to the transmission line. This would also allow for greater flexibility with regard to both complex circuit applications and device fabrication changes. The resultant memory system, therefore, would offer the possibility of substantially lower cost than if integrated cells were used. Moreover, advances in device technology made during the earlier part of this program made it possible to fabricate individual devices which were sufficiently small that the overall size of a cell, connected in the transmission line, would be comparable to the size of the integrated cell package.

The basic idea for such miniature devices is shown in Figure 4-4. The semiconductor pellet (Ge or GaAs) is soldered directly to a metal tab to form one connection to the diode. The upper connection is supported by means of a suitable insulator. Depending on the detailed fabrication techniques used, such a diode could be made .020 inch to .030 inch in diameter, and .010 inch to .020 inch in height. In order to fully evaluate this type of structure, two different approaches were taken.

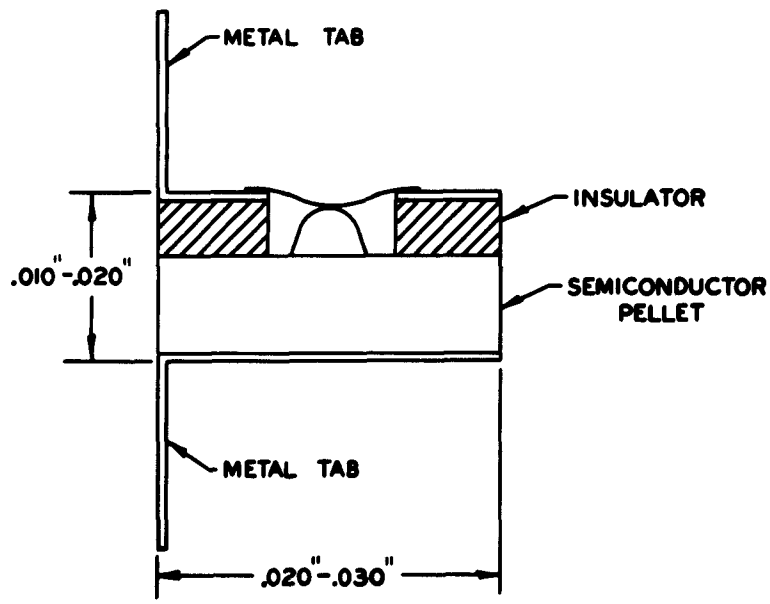


Figure 4-4. Miniature Tunnel Diode Structure [8]

The germanium tunnel diodes were made using a small ceramic washer as the insulator which supports the top connection. Since the ceramic must no longer completely enclose the semiconductor pellet and alloy dot (as in the conventional tunnel diode package), a much smaller size could be realized. Thus, the dimensions of the ceramic washer for this structure is only .025 inch O.D. x .010 inch I.D. x .005 inch in height. Both top and bottom surfaces of the washer are metallized and plated, and the washer is then brazed to a strip of kovar with a hole which is concentric with the washer hole. After gold-plating, this is soldered to the germanium pellet. Another gold-plated kovar tab is then soldered to the other side of the pellet. A tin dot containing 3% arsenic is then alloyed to the pellet, a screen connection is made, and the unit electrolytically etched in the usual way. The overall structure is quite small, being about .025 inch x .030 inch x .060 inch. Figure 4-5 shows a photograph of such a diode, as seen looking down at the screen connection.

Using this technique, 15 germanium tunnel diodes were made with electrical characteristics as shown in Table 4-1. These diodes all fall within a specification, also shown in Table 4-1, which is characteristic of slightly higher speed tunnel diodes than those used for the conventional memory subsystem. However, a perfectly acceptable memory subsystem could be made using such germanium tunnel diodes.

A different approach was used in making the gallium-arsenide tunnel rectifiers. Here, tin dots were first alloyed to the gallium-arsenide pellets. The pellets were then soldered to small gold strips, and a 0.2 mil gold wire then connected to the dot. The tab and wire were then welded to a small holding fixture (for ease in handling). An epoxy resin was then placed over the rectifier structure so as to leave only part of the alloy dot unprotected. After the epoxy hardened, the rectifier was electrolytically etched to specifications, and additional epoxy added to completely cover the alloy dot. The rectifier was then removed from the holding fixture (for this development, a transistor header was used). Figure 4-6 shows a photograph of this structure, as seen looking down at the wire lead. The overall dimensions of this device is about .020 inch x .020 inch x .040 inch.

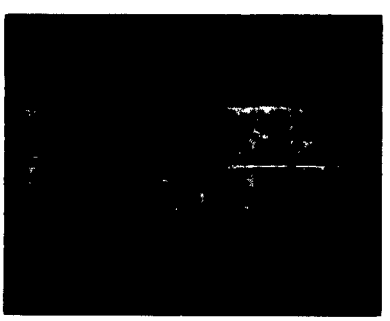


Figure 4-5. Microminiature Germanium Tunnel Diode [a]

TABLE 4-1
MICROMINIATURE GERMANIUM TUNNEL DIODES

Unit No.	I_p ma	I_v ma	E_p mv	E_v mv	E_b mv	C_v pf
1	3.05	0.29	65	305	510	4.8
2	2.95	0.24	64	295	495	3.8
3	2.95	0.23	64	305	475	2.4
4	3.0	0.25	63	300	475	3.5
5	2.88	0.245	63	295	485	4.9
6	3.0	0.235	59	295	495	5.4
7	2.90	0.25	64	290	500	2.5
8	3.12	0.30	64	305	485	2.2
9	2.95	0.25	64	295	495	3.0
10	3.15	0.30	63	310	490	3.8
11	3.05	0.27	63	310	480	1.9
12	3.05	0.27	63	295	485	5.0
13	3.05	0.29	63	300	490	2.0
14	3.10	0.21	65	315	510	5.0
15	2.90	0.27	61	290	480	3.1
Specification						
min	2.85	0.21	59	290	475	1.8
max	3.15	0.35	65	325	515	5.5

Figure 4-6. Microminiature Gallium-Arsenide Tunnel Diode [s]

Thirteen gallium-arsenide tunnel rectifiers were made in this way. Their characteristics, together with the tunnel rectifier specifications, are shown in Table 4-2. It was found that meeting these specifications, using this technique for making the rectifiers, was not especially difficult. In general, this technique was easier than the one using the ceramic support ring for the germanium tunnel diode. This technique has also been used successfully for germanium tunnel diodes.

In addition to the tunnel diode and tunnel rectifier micro-structures which were developed during the last quarter, an evaporated resistor on a .010 inch x .030 inch x .060 inch ceramic substrate was developed. The basic technology for this resistor was developed during the earlier phases of this program (where the substrate was the bottom of the memory cell package shown in Figure 4-2). However, a number of significant improvements were made during this quarter.

The ceramic substrate used for the resistor was designed to allow the tunnel diode and tunnel rectifier to be soldered directly to it. A "T" shaped metallization was deposited on one side of the substrate. This was connected to the other side at one end with an edge metallization obtained by solder dipping. The substrate was then gold plated. Figure 4-7a shows the back side (metallized) of the ceramic substrate. The scale is calibrated in hundredths of an inch.

Before depositing the resistor on the opposite side of the substrate, the ceramic was glazed with a pyrex frit coating. Resistor contacts were deposited at the ends of the substrate by evaporating chromium and gold. The use of evaporated contacts eliminated the instability and burnout problem of the earlier resistors, caused by the use of heavy solder contacts.

The resistor film (nickel-chromium) was evaporated as before, coated with silicon monoxide, aged at 150°C for four days, adjusted to value, and recoated with SLO. Resistance adjusting was accomplished by one of two methods. Either a diamond scribe, or an electric arc, was used to cut away a portion of the resistor film, thus increasing the resistance to the desired value. Both methods were successful, and superior to the air-abrader technique used previously. The resultant resistors met the electrical specifications listed below, and showed excellent life properties.

Size: .010 inch x .030 inch x .060 inch

Resistance: 2000 ohms ±2%

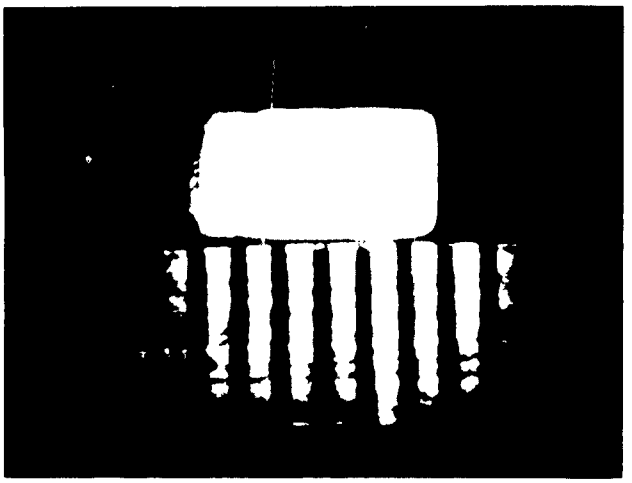
Temperature Coefficient: 50 ppm/°C maximum for 0 to 50°C

Noise: 0 db/decade maximum (i.e., 1 μ volt/volt/decade)

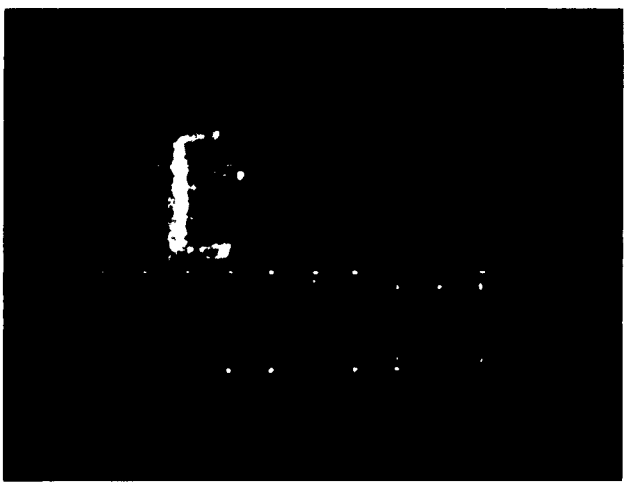
Life: Rated current (3 ma) applied continuously for 2,000 hours at 50°C with maximum change = ± 2%

TABLE 4-2
MICROMINIATURE GALLIUM-ARSENIDE TUNNEL RECTIFIERS

Unit No.	I_p (ma)	E_f @ 1ma (mv)	E_R @ 4ma (mv)	Capacitance (PF)
1	0.265	1120	200	1.5
2	0.50	1100	104	2.5
3	0.155	1130	215	0.80
4	0.100	1160	205	2.5
5	0.395	1060	213	1.4
6	0.190	1130	195	1.8
7	0.25	1030	215	1.8
8	0.22	1130	215	1.8
9	0.285	1130	207	2.0
10	0.255	1120	208	2.1
11	0.325	1070	205	1.1
12	0.40	1100	178	1.6
13	0.11	1120	212	1.3
Specification	<0.500	945-1155	<215	<2.5



(a) Metallized Region for Tunnel Diode Connection



(b) Resistance Region

Figure 4-7. Microminiature Resistor [5]

A photograph of the resistor side of the substrate is shown in Figure 4-7b. Table 4-3 shows the values for 15 resistors made in this way. Seven are within 2% of 2000 ohms, and 14 meet a 4% tolerance.

In addition to the effort devoted to the development of individual micro-components, some experiments were also performed to connect the tunnel diode and tunnel rectifier to the resistor, thus forming a memory cell. Using mechanical sample resistors (i. e., resistors which were electrically good, but out of specification), several memory cells were assembled with reasonable success. Soldering was accomplished using indium solder (melting point = 156°C), and a special micromanipulator jig for holding a fine-point soldering iron.

Table 4-4 shows the electrical characteristics of three units before and after interconnecting them. As shown, some changes in electrical characteristics did occur. However, it is believed that additional work on interconnection techniques would solve this problem. For example, laser welding techniques could be used to heat a very locallized region for a very short time, thus avoiding damage to the tunnel devices by excessive heating. Figure 4-8 shows a photograph of a memory cell. Also shown, for size comparison is a conventional tunnel rectifier.

TABLE 4-3
CERAMIC SUBSTRATE WITH THE RESISTOR

Unit	Resistance (ohms)
1	2043
2	1977
3	2073
4	2059
5	2056
6	1974
7	2014
8	1998
9	2052
10	2046
11	2000
12	2094
13	2020
14	2002
15	2080

Figure 4-8. Integrated Memory Cell (s)

TABLE 4-4
RESULTS OF INTERCONNECTION EXPERIMENT

	Before Mounting					After Mounting				
Tunnel Diodes Unit No.	I_p (ma)	I_v (ma)	E_p (mv)	E_v (mv)	E_f (mv)	I_p (ma)	I_v (ma)	E_p (mv)	E_v (mv)	E_f (mv)
1	1.7	0.20	74	290	530	1.46	0.09	70	300	520
2	2.5	0.60	76	250	470	2.10	0.44	75	248	400
3	1.79	0.20	60	280	465	1.79	0.21	60	260	430
Tunnel Rectifier Unit No.	I_p	I_v	E_f	E_{-R}		I_p	I_v	E_f	E_{-R}	
1	0.255		1090	205		0.245		1190	280	
2	0.202		1180	220		0.212		1170	224	
3	0.108		1130	220		0.100		1210	400	
Resistor Unit No.		Ohms					Ohms			
1		2470					2500			
2		640					640			
3		940					940			